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Design of a universal test platform for radiation testing of digital components

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THESIS

DESIGN OF A UNIVERSAL TEST PLATFORM FOR RADIATION TESTING OF DIGITAL COMPONENTS

by

Duane E. Amsler Jr.

September 1996

Thesis Advisor: Douglas Fouts

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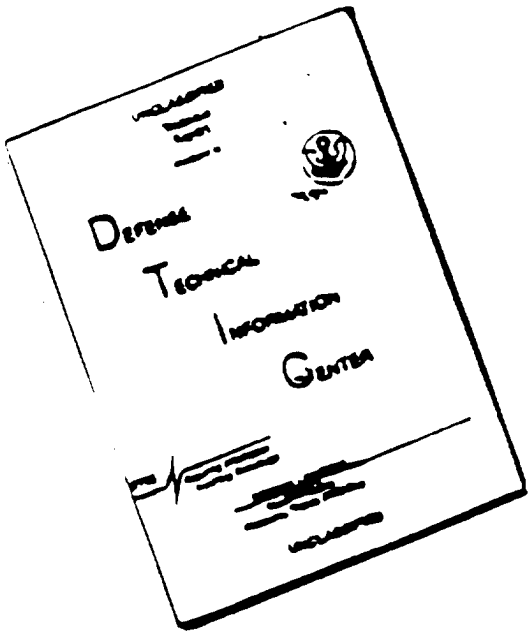

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In this research, programmable, microcontroller-based test hardware was designed, constructed, debugged, and programmed. The wire-wrapped board will be used to test two custom static random access memory (SRAM) chips, as well as other custom chips designed at the Naval Postgraduate School. Components for the test hardware were selected to allow prototyping with standard parts that can later be replaced with radiation hardened parts as budgets permit. Control of the test hardware is via a RS-232 serial interface, which allows remote control programming and monitoring of the test hardware and device being tested.

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I. INTRODUCTION

A. OVERVIEW

One of the major constraints in designing for the space environment is the ability of parts to withstand radiation. Radiation hardened (RAD hard) parts are typically reengineered designs of commercially available parts, which are adapted to a RAD hard fabrication process. Traditional designs are reworked to assure immunity to such radiation effects as latchup and single-event upsets (SEUs). The additional engineering and radiation hardened process significantly increases cost and time to market. Ongoing research at the Naval Postgraduate School is developing a process that should allow off-the-shelf gallium arsenide (GaAs) integrated circuits (IC) designs to be fabricated on specially prepared wafers that contain buried, low-temperature grown, GaAs buffer layers. The intent of the program is to run these specially prepared wafers through commercial GaAs wafer processing lines to create radiation-hardened ICs, without additional IC re-engineering and special IC processing steps.

The goal of this research is to create test hardware capable of testing ICs created using low-temperature (LT) GaAs wafers for functionality, as well as immunity to single-event upsets in a radiation environment. The original requirement was to test a Vitesse 256 X 4 static random access memory (SRAM), but additional requirements to test a Motorola 256 x 16 SRAM and a custom SEU detection IC were added. The test hardware is programmable through a RS-232 serial port and can be configured to read and write any desired data and address patterns for devices with up to 80 I/O pins.

Current work in this area is sparse. Oregon State University uses a basic 8051 design for teaching microprocessor basics and have developed very good monitor, which is used as part of this design. A previous thesis by Chris Mooney[1] address interfacing these two SRAMs to a satellite test board. The Mooney thesis design is only for these specific ICs and cannot be used independent of the satellite. This thesis creates a design that is capable of testing these two SRAMs, as well as a multitude of ICs, in a radiated environment.

B. THESIS ORGANIZATION

The goal of this thesis is to document the design, construction, testing, and programming of hardware that is capable of testing ICs in a radiation environment. To this end, the following organization will be followed. Chapter II will present an overview of the LT GaAs program, as

well as a brief overview of radiation effects. Chapter III discusses the various components selected and their basic operation. Chapter IV will provide a detailed discussion of the design and operation of the test hardware. Chapter V discusses the software involved to run the hardware, as well as the code for specific tests. Chapter VI presents conclusions, as well as potential future improvements and enhancements.

II. THE LOW TEMPERATURE GALLIUM ARSENIDE RESEARCH PROGRAM

A. OVERVIEW

One of the most significant costs in developing systems to operate in the space environment is that of radiation hardening electronic components. These RAD hard ICs are specially engineered to a set of design rules that apply to a specific fabrication process. As a result of this additional engineering, special fabrication processes, and relatively low demand, RAD hard devices are typically 100 times more expensive that their commercial counterparts.

Some of the radiation effects of digital ICs include device degradation, latchup, and single event upsets. Degradation is caused by both the depositing of charge within the device and actual crystal lattice damage. Both will cause the device specifications to change and may eventually result in total failure. Latchup is a condition where a temporary short from power to ground is caused by the interaction between a transistor, a charged particle, and parasitic circuitry on the IC. If this does not destroy the device or power supply, the circuit may be powered down and restarted. A single-event upset is a condition where a particle passes through a transistor or memory element and causes the associated bit to flip, producing a data error. After this temporary data upset, the device will continue to function normally.[2]

To mitigate the effects of radiation, a number of technologies have been developed for complementary metal oxide silicon (CMOS) ICs which require the reengineering of commercial parts, as mentioned above. For high-speed applications gallium arsenide (GaAs) circuits have proven to be superior to emitter coupled logic (ECL) and bipolar complementary metal oxide silicon (BiCMOS) in resistance to degradation and latchup. However GaAs SEU rates are four to seven times greater than most Department of Defense (DoD) requirements. A great deal of research has been conducted at the Naval Postgraduate School and elsewhere to find a method of improving the SEU characteristics of GaAs. One such research effort is called Low Temperature Gallium Arsenide (LT GaAs), where a buffer layer of gallium arsenide is grown at low temperatures, around 200° C, as opposed to the 600°C that is typically used for gallium arsenide processes. It has been shown that this low-temperature buffer layer eliminates SEU effects in GaAs ICs. If successful, this process will allow specially prepared wafers to be run through

traditional GaAs processing steps with commercially developed mask sets. This will significantly reduce the cost of developing high-speed, low-power circuits for space-based applications.[3]

To this end, some LT GaAs wafers were run through commercial processes at both Vitesse and Motorola. Vitesse produced a 256 X 4 SRAM and Motorola produced a 256 X 16 SRAM, both with existing commercial mask sets. These two memories need to be tested for both functionality and resistance to single-event upsets. To this end, the design of a board capable of performing such tests is examined in this thesis. The following two sections detail the electrical characteristics and pin-outs of the LT GaAs chips to be tested.

B. VITESSE 256 X 4 SRAM

The Vitesse SRAM was produced with their commercial mask set and was packaged in a 28-pin dual flat pack. This SRAM operates in the 10 ns range and has separate data inputs and outputs. The overall interface includes 8 address, 4 data in, 4 data out, read, write, and two chip select pins, one active high and one active low. Vitesse no longer produces this SRAM as an off-the-shelf part and a third party package was needed to package the die, which is the reason for the somewhat unconventional pin-out of the package. Figure 1 shows the package pin out diagram of the Vitesse SRAM.

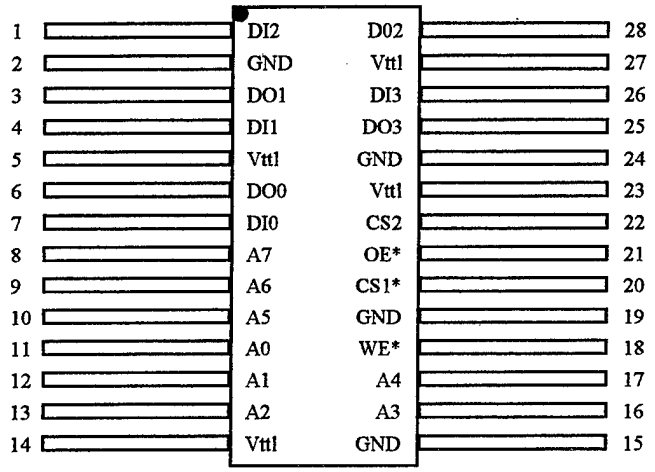

Figure 1: Vitesse 256 X 4 SRAM

C. MOTOROLA 256 X 16 SRAM

This SRAM mask set is part of a library for digital signal processing (DSP) IC development and does not have off-chip drivers, therefore requiring additional support circuitry. Input and output voltage levels are 0 and 0.9 to 2.0 volts. Thus, voltage reduction is required for

the inputs and amplification for the outputs. The voltage reduction can be accomplished using two diodes with a resistor, and the amplification can be performed with high-speed comparators. This interface circuitry is being developed by another student at the Naval Postgraduate School.

The interface of the chip, which drives the test setup on this board, consists of 8 address, 16 data in, 16 data out, write enable, and clock lines. There are also multiple power and ground connections for the clock buffers, output drivers, and memory elements. The manufacture's data sheet states that the address and write enable lines should be changed during clock low. On a clock high, the address is decoded and data is written if the write line is enabled, or read if the write line is low.

This chip is mounted in a 68-pin leaded chip carrier, again a third party package as this is not an off-the-shelf SRAM at Motorola. Figure 2 shows the pin outs of the 68-pin package.

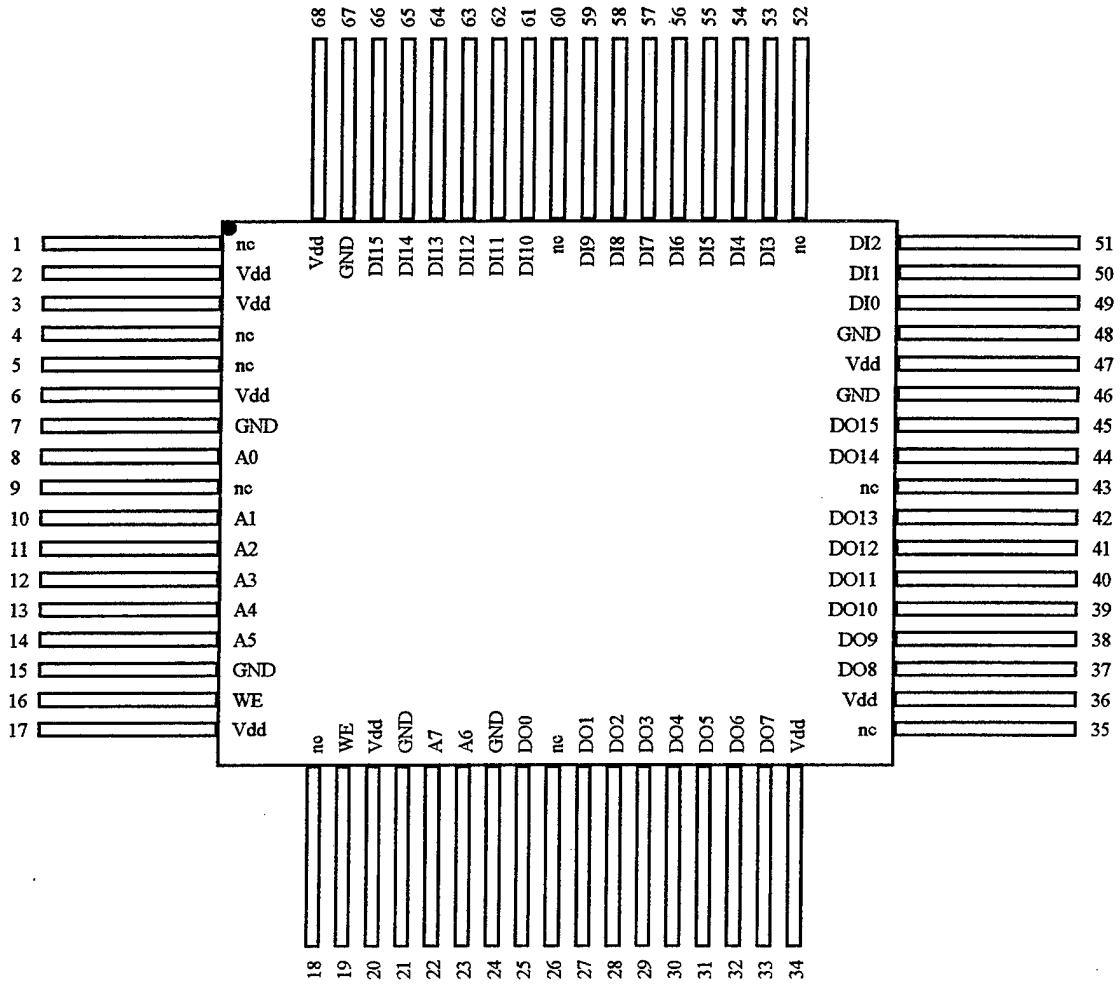

Figure 2: Motorola 256 X 16 SRAM

III. COMPONENT SUMMARY

A. OVERVIEW

The intent of this project was to design and build test hardware that would allow functional and radiation testing of a Vitesse 256 X 4 SRAM fabricated with the LT GaAs process. The test fixture is required to be portable and capable of interfacing to a laptop computer via a RS-232 serial port. The original considerations for designs were as follows:

RS-232 controlled logic

Microprocessor Based Design

Microcontroller Based Design

Using a single, RS-232 I/O port design would have required a number of registers to control the experiment. For the Vitesse chip, which is a 256x4 SRAM, two 8-bit registers would have been needed to control chip inputs (8 bits for address, 4 bits for data, and 4 bits for control signals CS1, CS2, Write Enable, and Output Enable), and a 4-bit register would have been required for reading data out. This design, although relatively simple, is very limited and only allows for testing of this specific chip. Furthermore, addressing all the registers would require additional hardware and operation would be very slow. To test a more complex chip, other circuitry must be added, and the software correspondingly changed. Ultimately, this design methodology was scrapped due to its limited utility.

The microprocessor-based design was considered, along with the microcontroller-based design, and it was determined that a microcontroller was more flexible and capable due to the built-in features of most microcontrollers, which usually include serial support, on-board ROM, and built-in I/O.

Once it was determined that a microcontroller-based design was to be used, the question of which microcontroller arose. Since one of the design considerations was to have a test fixture that could be used in a radiation environment, the choice was narrowed down to 3 or 4 options. Ultimately, the United Technologies UT69RH051 was chosen for its compatibility with the 8051 family of microcontrollers. The 8051 family has a wealth of development tools available, which greatly aided in the development of this system.

B. SUMMARY OF VLSI COMPONENTS

Based on the choice of the UT69RH051 as the controller for the design, the following components are required. Data sheets for the following components are available in Appendix C. The first part number is the RAD hard version and the number in parenthesis is the commercial version for each IC.

1. UT69RH051 Microcontroller (i8051)

The UT69RH051 is a RAD Hard version of the Intel i8051 series of microcontrollers. This is a 40-pin device consisting of four 8-bit ports (ports 0-3), with additional pins for clock (XTAL1and XTAL2), address latch enable (ALE), program store enable (PSEN*), external access enable (EA*), and reset (RST). Port 0 is a multiplexed port providing both the lower byte of the address and the data byte. The ALE line is asserted when the low order address byte is on port 0. The PSEN* serves as the read signal for the program memory space, while the EA* is an input indicating whether to use internal ROM (not available on the UT69RH051) or an external ROM. The XTAL1 and XTAL2 lines are used to provide timing control. The XTAL1 input can be used alone if an oscillator is used to generate timing, otherwise both XTAL lines are used with a simple crystal and capacitor combination. Port 1 may be used for special purpose I/O. However, it is used here as a basic 8-bit I/O port. Port 2 provides the high-order address byte. Port 3 provides for general I/O control to include the read (RD*) and write (WR*) signals to memory and the serial transmit (TXD) and receive (RXD) lines to the RS-232 interface.

2. MAX233

The MAX233 is a multi-channel RS-232 driver/receiver that converts serial data between 0 and +5 V (TTL) and ±10 V (RS-232). This chip has the added benefit of not requiring any additional power supply beyond the +5 V on which the chip and board operate. The only pins of interest are Tin, Tout, Rin, and Rout, which are the transmitter and receiver inputs and outputs. Other interface pins are tied together per the data sheet.

3. HS-82C55ARH (82C55)

The HS-8255ARH is a general-purpose, programmable, I/O device with 24 I/O pins organized as ports A, B, and C. Ports A and B are 8-bit ports and can each be programmed as either byte input or byte output. Port C is divided into two 4-bit I/O groups, each of which can be programmed as input or output. The port C lines can be configured to be individually set or reset

in output mode, which aids in the simulation of control signals. For interfacing, chip select (CS*), write (WR*), read (RD*), two address lines, and 8 data lines (D0-D7) are provided. A RESET pin is also provided to allow the 8255 to be started in a known program state. Lines A0 and A1 specify ports A, B, C, or control-word access.

4. UT28F64 (AM2764A)

The UT28F64 is a RAD hard 8Kx8 PROM manufactured by United Technologies. This PROM will operate on 5 V and has an access time of 35ns. The interface pins are 13 address lines, 8 data lines, 3 control lines, power and ground. The three control lines are output enable (OE*), which is essentially a read line, chip select (CE*), and a programming line (PE*), which is asserted during programming and held high during operation. The 2764 has one additional pin, Vpp (pin 1) which is used during programming and is tied high for operation.

5. UT67164 (61C64)

This is an 8Kx8 RAD hard SRAM with a 55 ns access time. The UT67164 is also SEU hardened but is contained in a 600 mil package, as opposed the standard 300 mil used for standard SRAM's, as well as the 61C64 used on the prototype board. Interface pins are identical to the PROM with the omission of the program lines.

C. SUMMARY OF MSI COMPONENTS

1. UT54ACS08 (74HC08)

The UT54ACS08 is a RAD hard version of a quad 2 input AND gate.

2. UT54ACS138 (74HC138)

The UT54ACS138 is a RAD hard version of a 3-to-8 line decoder with three enable inputs, one active high, and 2 active low. When the proper input conditions are met, a single output line will go low indicating that it is selected, all other outputs remain high.

3. UT54ACS245 (74HC245)

The UT54AC245 is a tri-state octal bus transceiver. It is RAD hard and has an 8-bit A bus, an 8-bit B bus, an enable line, and a direction control line. As with the other devices, if the enable line is inactive (high), both buses are in the high impedance state. If the enable is asserted, data is transmitted from the A to the B side if the direction input is high, otherwise data is sent from the B to the A side.

4. HCS573MS (74HC573)

The HS573MS is an octal latch with tri-state outputs and is RAD hard. The 573 has a broadside configuration where all inputs are on one side and all outputs are on the other. The interface pins consist of 8 input bits and 8 output bits, as well as an output enable (OE*) and a latch enable (LE). When output enable is not asserted (high), the outputs are in the high impedance state. When latch enable is high, the latch is transparent. When the latch enable is asserted, the input data at that moment is held on the outputs until the latch enable goes high again.

5. HCS574MS (74HC574)

The HCS574MS is a RAD hard broadside octal D flip-flop with tri-state outputs. It has 8 input and 8 output pins, as well as an output enable (OE*) and a clock (CP) pin. On a low-to-high transition of the clock line, data on the inputs is stored and available on the outputs until the next low-to-high transition (assuming outputs are enabled).

D. DIGITAL COMPONENT ELECTRICAL REQUIREMENTS

The majority of electrical components are available in both CMOS and TTL compatible versions. For driving external components, HCT (high speed CMOS supporting TTL I/O levels) components are used, otherwise HC (high speed CMOS) components are used. Port 0 of the 8051 is capable of driving 4 TTL loads or a virtually unlimited number of CMOS loads (as the typical CMOS load draws an order of magnitude less current than TTL loads). The remainder of the 8051 ports will sink 3.5mA or source 0.3 mA, which is more than sufficient to drive 10 CMOS loads. The bus transceivers at the outputs of the XX245 will sink and source 12mA, which is sufficient to drive virtually any device to be tested. The outputs of the 8255 will sink and source 2mA, which is sufficient to drive most control lines. Further interface limitations will be discussed in Chapter V. A summary of the output currents of the devices used are shown in Table 1.

Component	I_{OH} (mA)	I_{OL} (mA)
8051 Port 0	-7.0	7.0
8051 Port 1,2,3	-0.3	3.5
MAX232/233	-1.0	3.2
HS-82C55ARH	-2.0	2.0
UT28F64	-.4	4.0
UT67164	-.4	4.0
UT54ACS08	-8.0	8.0
UT54ACS10	-8.0	8.0
UT54ACS138	-8.0	8.0
UT54ACS139	-8.0	8.0
UT54ACS245	-12.0	12.0
HC573MS	-7.2	7.2
HC574MS	-7.2	7.2

Table 1: Summary Of Component Pin Currents

E. DISCRETE COMPONENTS

1. Crystal Oscillator

A crystal oscillator with a frequency of 7.3728 MHz was used to provide timing input to the microcontroller. This seemingly odd frequency aids in ensuring the baud rates on the serial port fall within standard ranges such as 4800, 9600, etc. The microcontroller will run on any frequency from 2 - 20 MHz.

2. Capacitors

a. 10 μF

A 10 μF capacitor is used in conjunction with a resistor to generate a time delay for the reset line of 8051 and 8255 on power-up. This value is recommended in the data sheets.

b. 1μF

Four, 1 μF capacitors are used with the MAX232 to provide ±10 V DC using the charge pump circuitry built into the device. These will not be required on the production board as the MAX233 will be used, which does not require external capacitors.

c. .1μF

These capacitors are used for decoupling, that is providing a momentary source of current when ICs switch, providing voltage stability.

3. Resistors

A 8.2KΩ resistor is used in conjunction with a capacitor to provide a time delay for the reset line of both the 8051 and the 8255 on power-up. This ensures the board starts in a known state, and is recommended on the data sheets.

F. CONNECTORS

1. 40 Pin Header

Four, 40-pin headers are used to provide an interface with the device to be tested. The pins are set up in a 2 X 20 grid with 100 mil spacing.

2. 25-pin sub-D

A 25-pin, sub-D, male connector is used to interface the board with a standard serial RS-232 port of a laptop computer.

IV. DESIGN ANALYSIS

A. OVERVIEW

A detailed description of the universal test platform's design and operation is provided in this section. The goal is to provide a stand-alone document that fully explains the wiring and operation of each section of the design.

B. SERIAL INTERFACE

The first task was to create an interface with the outside world using a RS-232 serial interface. The actual serial connection itself was rather easy in that this basic function was built into the microcontroller. The key part of this interface was to convert the TTL-level serial signals to the RS-232 levels. This could have been accomplished using one of the two major families of RS-232 drivers. The first is the 1488/1489 line driver/receiver combination. Both 148X ICs require ±12 V, which is not required elsewhere in this design. This choice also requires two IC packages, whereas the MAX232/233 family requires only one.

As this is a relatively simple serial connection, with only a transmit line(TXD) and a receive line(RXD), only one line driver and receiver are required. Maxim makes a family of line drivers and receivers on the same chip with the added benefit of requiring only a +5 V supply, instead of the ±12 V that is typically required of line drivers. This family of chips uses a technique called *dual charge-pump voltage conversion*, which uses capacitors to generate the ±10 V required for the RS-232 line drivers. The two devices used in this research are the MAX232, which use external capacitors, and the MAX233,which has internal capacitors and therefore requires less board space. The MAX232 was used on the wire wrapped board, primarily because of its availability early in the design process. For the production board, the MAX233 is used.

1. MAX232

The MAX232 requires four external 1 μF capacitors, as well as power and ground for support circuitry. The functional portion of the MAX232 contains two line drivers and two line receivers, of which one each is used. The wiring diagram for the MAX232 is shown in Figure 3.

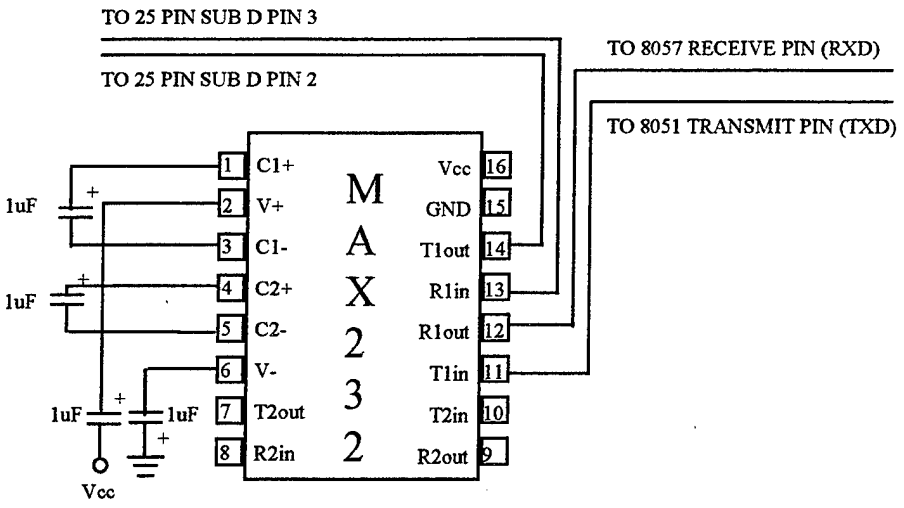

Figure 3: MAX232

2. MAX233

The MAX233 is an improvement upon the MAX232 in that it requires only +5 V and ground, with no external capacitor requirement. It also contains two line drivers and two line receivers and is wired as shown in Figure 4.

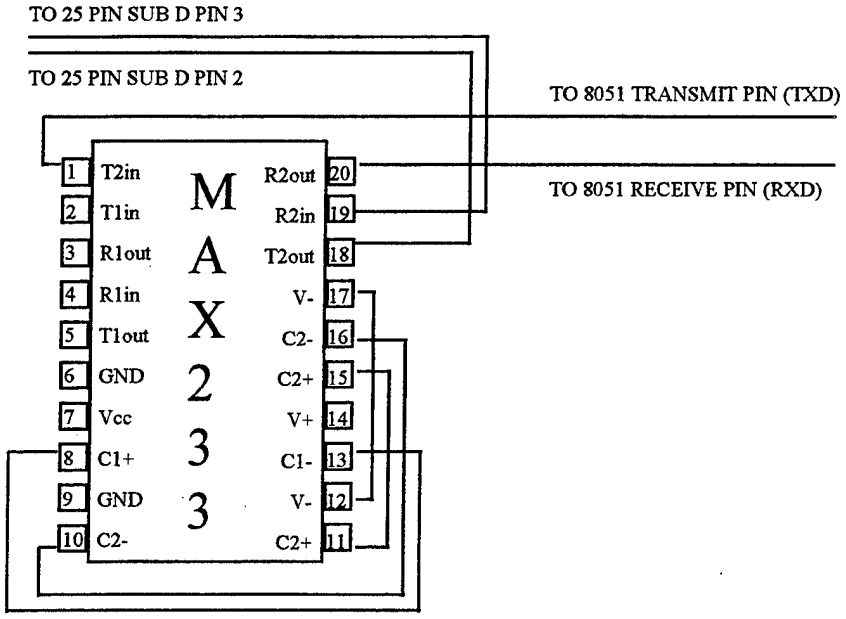

Figure 4: MAX233

3. Serial connector

The output of the line driver and the input of the line receiver are wired to a standard, male, 25-pin, sub-D connector, as shown below in Figure 5. The line driver output is connected to pin 3 of the connector (received data for DTE in the RS-232 standard), and the line receiver is connected to pin 2 of the connector (transmitted data). Pin 7 (signal ground) is connected to ground.

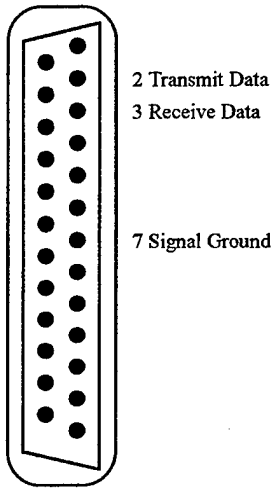

Figure 5: RS-232 Connector (minimal)

4. Overall Serial Subsystem

The input of the line driver is connected to the serial transmit (TXD) line of the microcontroller and the line receiver output is connected to the serial receive (RXD) line of the microcontroller. The MAX23X receive data in (Rin) and transmit data out (Tout) are wired in accordance with the RS-232 standard, as shown above. The complete communications subsystem is shown in Figure 6.

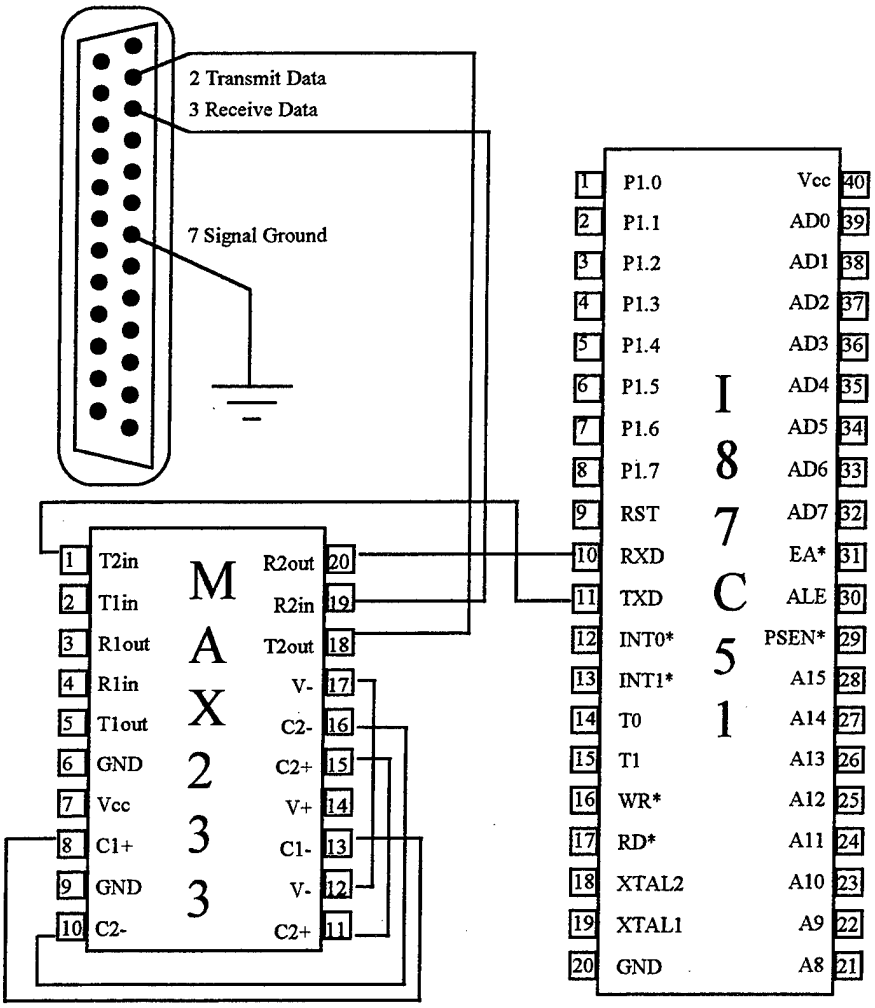

Figure 6: Complete Serial Subsystem

C. TIMING GENERATION

The timing generation for this system can use one of two methods, depending upon what the desired timing source is. The two choices are to use a crystal or a R/C oscillator. The difference is accuracy versus complexity and both have been used in developing the prototype board. The R/C oscillator was dismissed because it is not stable enough for serial-line baud-rate generation. When the R/C oscillator is used, the output is wired to pin 19 (XTAL1) of the microcontroller.

When a crystal is used, two additional capacitors are required, providing parallel resonance for the fundamental response mode of the crystal. When this configuration is used, the crystal is wired to pins 18 and 19 (XTAL2 and XTAL1) of the microcontroller and both pins are

grounded through capacitors, as shown in Figure 7. This method was chosen because of its simplicity and the relative tolerance crystals and capacitors show to radiation effects.

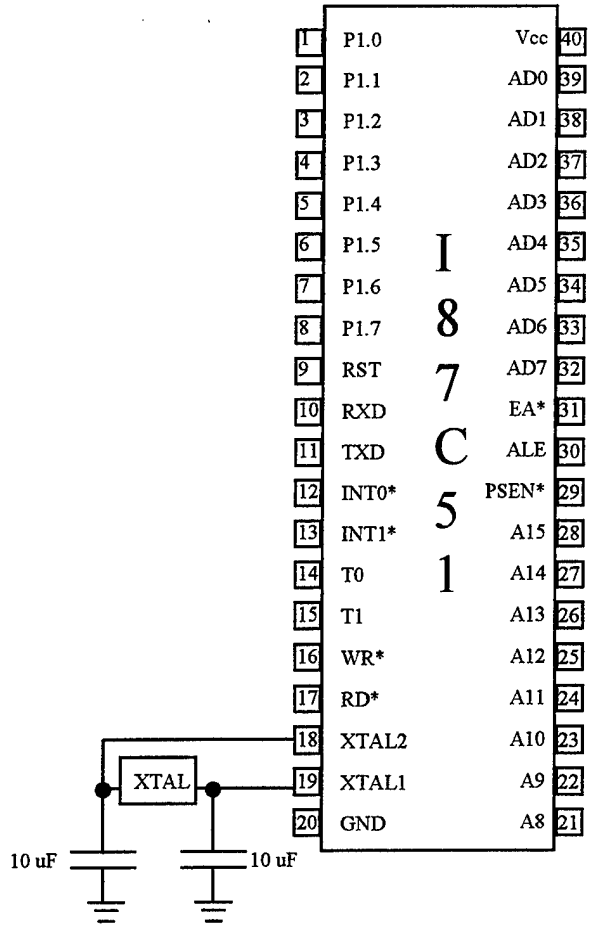

Figure 7: Timing Subsystem

D. MEMORY INTERFACE

1. Overview

The memory subsystem is also relatively straight forward, the most difficult part of which is latching the low order address-byte so it is available while the data-byte is on the output port. The memory space is divided into eight, 8K blocks within the 64K memory space. The basic memory layout is shown in Table 2.

MEMORY LOCATIONS	USE
0000H-1FFFH	ROM SPACE
2000H-3FFFH	RAM 1 SPACE
4000-5FFFH	RAM 2 SPACE (PRODUCTION BOARD)
6000-7FFFH	BOARD CONTROL SPACE
8000-9FFFH	TEST SPACE 1
A000-BFFFH	TEST SPACE 2
C000-DFFFH	TEST SPACE 3
E000-FFFFH	TEST SPACE 4

Table 2: Memory Map

2. XX573

Port 0 of the 8051 is multiplexed and used for both the low-order address byte and the data byte to be written or read. Therefore, the address byte must be stored and held for use during the memory access cycle. This is accomplished easily with either a XX373 or XX573 latch. The XX573 was chosen for its broadside configuration, where all input pins are on one side of the package and all output pins are on the opposite side of the package. This makes it easier for both wire wrapping and printed circuit board production, where it is desirable to keep trace and wire lengths to a minimum.

The support pins on this chip are straight forward: power, ground, output enable (OE*), and latch enable (LE*). The output enable was wired low, allowing the address to always be available after latching. The latch enable line is wired to the address latch enable (ALE*) line of the microcontroller, an obvious choice.

3. XX138

The XX138 is used to partition the 64K address space into eight, 8K blocks. The support pins are: power, ground, and 3 enable lines. In this design, all enable lines are asserted, allowing the selected partition to be active as long as the upper three address bits indicate that partition.

4. XX08

The XX08 is used to combine the program store enable (PSEN*) and read (RD*) lines. This is a recommendation in many application notes [4,5] and allows the RAM to be used as both program and data memory. This facilitates the downloading of code into the RAM, which can then be run as a program. This eliminates the need to program a PROM every time a change is made in a program and allows for easy code modification with a simple monitor program. The complete memory interface is shown in Figure 8.

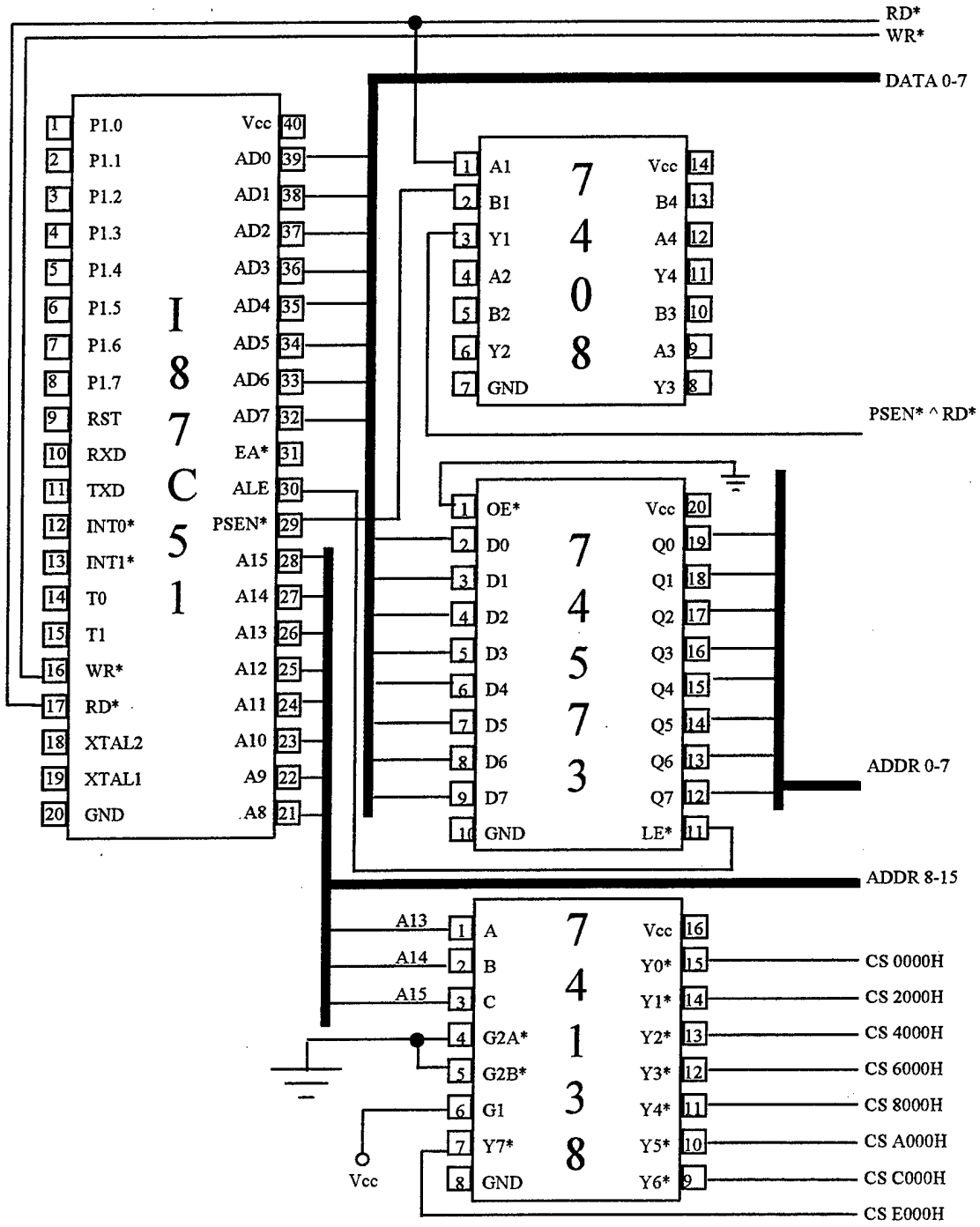

Figure 8: Memory Interface

E. MEMORY

1. PROM (UT28F64)

The PROM interface is very straight forward. The data lines are wired directly to port 0 of the microcontroller. The low-order byte of the address is latched by the XX573, therefore address lines 0-7 are wired to the latch. The 5 high-order address bits are wired to the microcontroller address lines on port 2. The remaining pins to be interfaced are the chip select (CS*), read (RD*), program (PGM), and program voltage (Vpp) lines. The PROM is designed to occupy the first 8K partition of the memory space and is therefore wired to the Y0 output of the XX138. The read line could be wired to either the read (RD*) line of the microcontroller or to the output of the XX08. Here, the output of the XX08 was chosen to minimize the lines wired directly to the microcontroller. The program and program voltage lines are wired high, as this design does not provide for programming the PROM. The PROM interface is shown in Figure 9.

2. SRAM (UT67164)

The SRAM interface is very similar to that of the PROM. The four support pins are the read (RD*), write (WR*), chip select 1 (CS1*), and chip select2 (CS2) lines. The write line is wired directly to the microcontroller and the read line is wired to the XX08 to allow the SRAM to act as both program and data memory space. The chip select 1 line is wired to the Y1 output to configure the SRAM as the second 8K partition. The chip select 2 line is not needed and is, therefore, wired high to allow only the chip select 1 line to activate the SRAM. The address and data lines are wired the same as for the PROM. Only one 8K SRAM is implemented on the prototype board. The basic interface is shown in Figure 9.

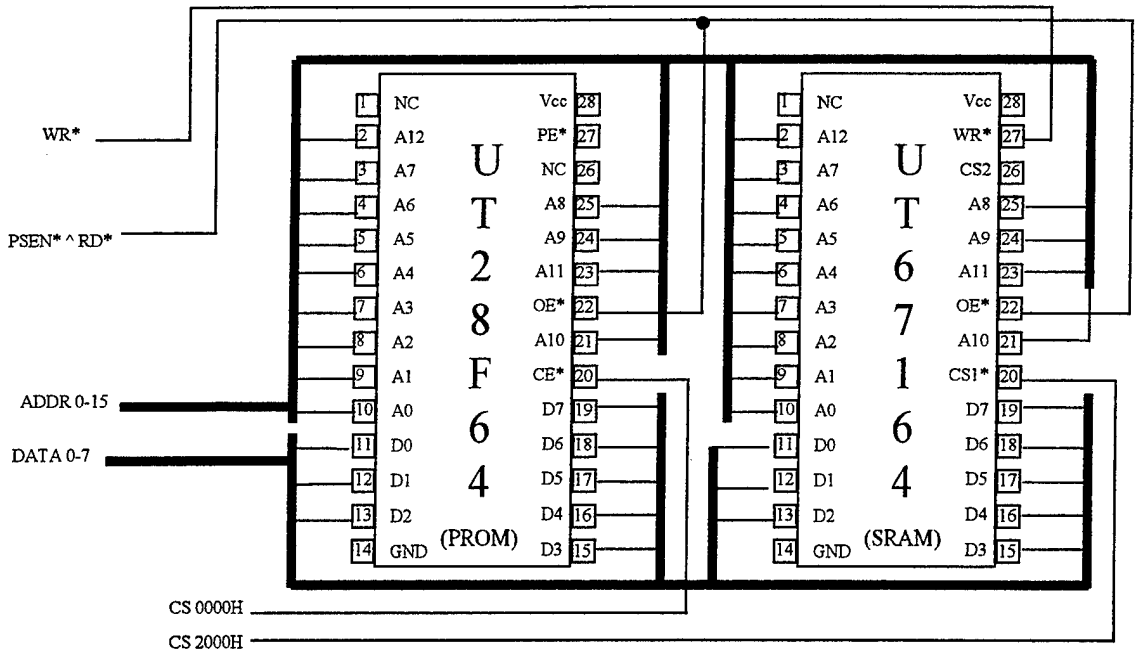

Figure 9: Memory Subsystem

F. PERIPHERAL INTERFACE

This section provides for additional I/O to interface with the device to be tested. Table 3 shows the memory map of the peripheral interface control space.

MEMORY LOCATION	USE
6000-6003H	8255 #1
6007-6007H	8255 #2
6008-600BH	8255 #3
600C-600FH	8255 #4
6010H	LATCHED BYTE 0
6014H	LATCHED BYTE 1
6018H	LATCHED BYTE 2
601CH	LATCHED BYTE 3

Table 3: Peripheral Memory Map

1. XX138

The XX138 is used to further subdivide the lower 32 bits of memory partition 3 (6000H-7FFFH) into 4-bit units. This is done to keep all the control board control functions within partition 3, allowing a 32K memory space for the device under test. The control inputs to this device are three address lines and three enable lines. The address lines are wired to address bits 2 to 4 of the XX573 latch, creating eight, 4-bit blocks. These blocks repeat every 32 addresses within memory partition 3 (6000H-7FFFH). The additional circuitry required to fully decode this address space is not implemented in this design.

2. 8255

The 8255 interface methodology is similar to that of a simple RAM. There is an 8-bit data bus and a 2-bit address bus along with read (RD*), write (WR*), chip select (CS*), and reset (RESET) lines. The data byte is wired to the microcontroller data bus, while the two address lines are wired to the lowest 2 bits on the memory-interface XX573 latch. The read, write and reset lines are all wired directly to their counterparts on the microcontroller. The remaining line to be interfaced is the chip select, which is controlled by the output of the XX138 that selects which 8255 is to be addressed. The first four outputs of the XX138 (Y0-Y3) select one of the four 8255s on the production board, or one of the two 8522s on the wire-wrapped board. The 8255s I/O interface has a total of 24 bits, which is arranged as three 8-bit ports. The address pins(A0,A1) select between ports A, B, C, and the control word. The three I/O ports are wired to the 40-pin connectors, allowing for control of the device to be tested. The 8255 interface is show in Figure 10.

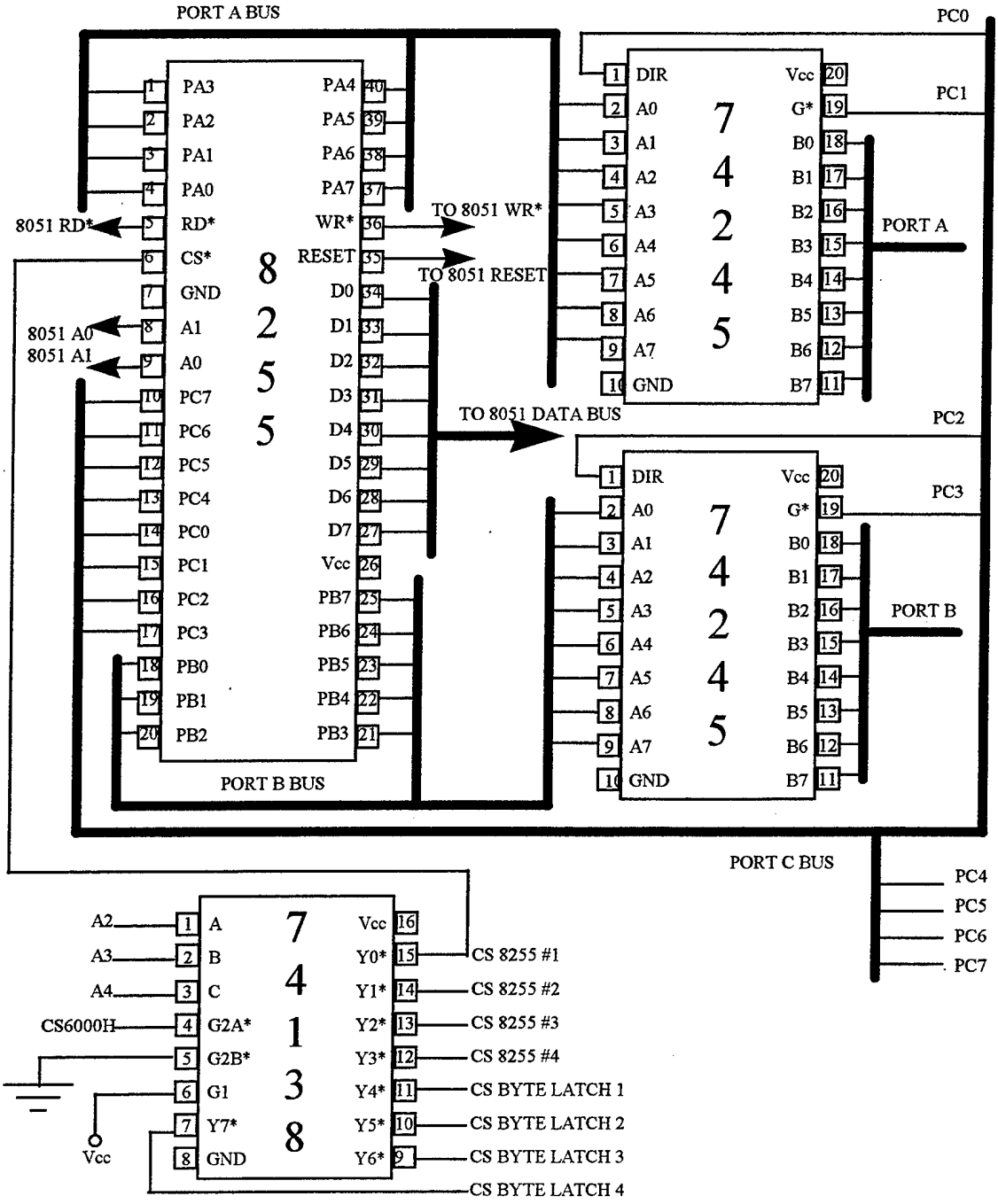

Figure 10: 8255 Interface

G. LATCHING / READING 32 BITS

To allow this device to test other ICs with data buses wider than 8 bits, a technique had to be developed to allow an eight-bit microcontroller to read multiple bytes. The method used here latches up to 32 bits of data, then reads the values a byte at a time from the control space.

1. XX574

The purpose of the XX574 used here is two fold, it allows for latching the data as well as acting as a tri-state buffer. The XX574 flip-flop was chosen because storage is desired on transitions, not simply on levels, as with the XX573 latch. The control lines of the XX574 consist of an output enable (OE*) and a clock input (CLK). When the CLK signal transitions from low to high, the data on the inputs is stored in the flip flops. The logic to control the clock line is discussed below. When a control space read is initiated, the output enable is activated and the stored data appears on the data bus.

2. XX08

The XX08 provides the input clock to the flip-flops when a specific set of circumstances is present, mainly when A15 is high and the read line transitions from low to high.

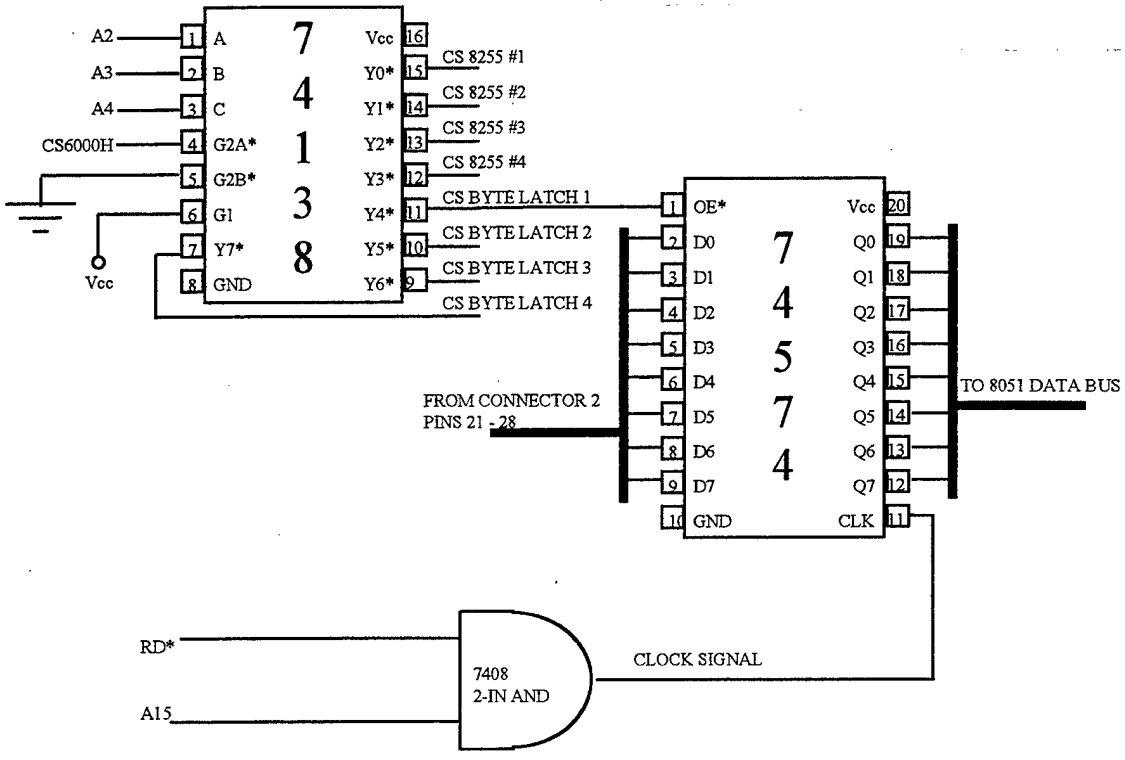

Figure 11: Byte Latch Circuitry

3. Word latch

To read 32 bits, all data bits of the device under test are stored at one time and are then read a byte at a time as part of the control space. A read from the test data space (upper 32K) will cause 32 bits of data to be clocked into the XX574s (16 bits on the prototype board). These bytes can then be read as part of the control space at addresses 6010H, 6014H, 6018H, and 601CH, as determined by the XX138 described in the peripheral interface section.

H. RESET

The reset circuitry is relatively straight forward, a switch with a capacitor and resistor to provide an appropriate delay, as specified in the applications notes. A diagram of this circuit is shown in Figure 12.

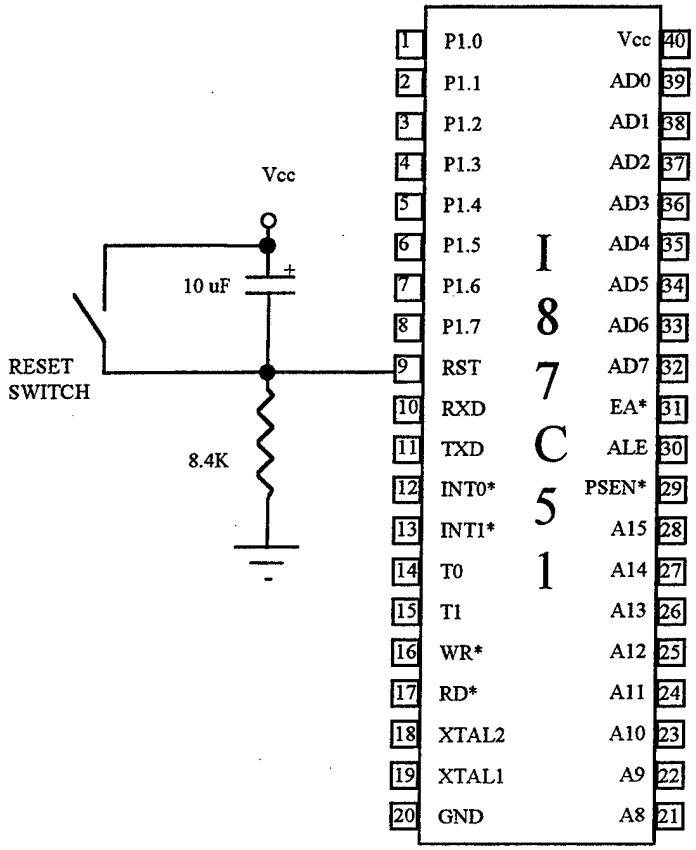

Figure 12: Reset Circuit

I. EXTERNAL CONNECTORS

1. RS-232

The connection to the outside world is through a 25-pin, sub-D, male connector, which is compatible with most standard computer serial interfaces. There are only three pins used, thus the protocol is fairly simple. Pin 7 is used for signal ground and pins 2 and 3 are used for transmit data and receive data, respectively.

2. Test Interface

The external connectors are 40-pin dip headers which are broken down by functionality. Connector 1 is the microcontroller bus interface. Connectors 2 and 3 each contain 16 bits of programmable I/O and a 16-bit latch capability, as well as 4 control bits. Connector 4 provides 32 bits of programmable I/O and some additional bit control lines.

a. connector 1

Connector 1 contains all the necessary lines to connect a device with an address space of up to 32Kb and an 8-bit data word. Also provided are 8 bits that can be programmed as an input or output byte. The specific signals include 16 address bits, 8 data bits, 8 I/O bits, and 4 chip selects, along with read, write, power and ground. Table 4 shows the specific pin arrangements. This connector is fully implemented on the prototype board. All signals use TTL levels and will drive TTL loads.

b. connector 2

Connector 2 contains two bytes that may be configured as either input or output, as well as two bytes capable of being latched by the control board. Also provided is a group of 4 bits that can be individually set and cleared, or serve as a 4-bit I/O port. The details are shown in Table 5 and are fully implemented on the prototype board.

c. connector 3

Connector 3 is designed to be implemented on the production board and is not on the prototype board. These signals are similar to what is provided on connector 2 and makes it possible to test a 32-bit memory device. The details are shown in Table 6.

PIN	FUNCTION	PIN	FUNCTION
1	DATA 0	21	ADDRESS 0
2	DATA 1	22	ADDRESS 1
3	DATA 2	23	ADDRESS 2
4	DATA 3	24	ADDRESS 3
5	DATA 4	25	ADDRESS 4
6	DATA 5	26	ADDRESS 5
7	DATA 6	27	ADDRESS 6
8	DATA 7	28	ADDRESS 7
9	POWER (+5V DC)	29	GROUND
10	I/O 0 (FROM PORT 1)	30	ADDRESS 8
11	I/O 1	31	ADDRESS 9
12	I/O 2	32	ADDRESS 10
13	I/O 3	33	ADDRESS 11
14	I/O 4	34	ADDRESS 12
15	I/O 5	35	ADDRESS 13
16	I/O 6	36	ADDRESS 14
17	I/O 7	37	ADDRESS 15
18	CS A000-BFFFh	38	READ*
19	CS C000-DFFFh	39	WRITE*
20	CS E000-FFFFh	40	CS 8000-9FFFh

Table 4: Connector 1

PIN	FUNCTION	PIN	FUNCTION
1	8255 #1 PORT A I/0 0	21	T/S DATA IN 0
2	I/O 1	22	T/S DATA IN 1
3	I/O 2	23	T/S DATA IN 2
4	I/O 3	24	T/S DATA IN 3
5	I/O 4	25	T/S DATA IN 4
6	I/O 5	26	T/S DATA IN 5
7	I/O 6	27	T/S DATA IN 6
8	I/O 7	28	T/S DATA IN 7
9	8255 #1 PORT B I/O 0	29	T/S DATA IN 8
10	I/O 1	30	T/S DATA IN 9
11	I/O 2	31	T/S DATA IN 10
12	I/O 3	32	T/S DATA IN 11
13	I/O 4	33	T/S DATA IN 12
14	I/O 5	34	T/S DATA IN 13
15	I/O 6	35	T/S DATA IN 14
16	I/O 7	36	T/S DATA IN 15
17	8255 #1 PORT C I/O 4	37	
18	I/O 5	38	
19	I/O 6	39	
20	I/O 7	40	

Table 5: Connector 2

d. connector 4

Connector 4 is designed to be implemented on the production board and is not on the prototype board. These signals provide additional I/O lines that may be used to drive a 32-bit address bus on larger devices being tested. Details are shown in Table 7.

J. TIMING ANALYSIS

The overall timing of components for this design is straight forward, as all timing is synchronous. Analyzing the memory timing constrains of the 8051 shows that time from a read low to data valid must be within the limits of Equation 4.1.

$$t_{RLDV} = 5t_{CLCL} - 165ns \qquad \text{Equation 4.1}$$

Here t_{CLCL} is the clock period low transition to low transition. Operating the 8051 at a maximum clock rate of 20MHz, t_{CLCL} is 50ns and t_{RLDV} is 85 ns. For the read and write pulse widths, Equations 4.2 and 4.3 apply.

$$t_{RLRH} = 6t_{CLCL} - 100ns \qquad \text{Equation 4.2}$$

$$t_{WLWH} = 6t_{CLCL} - 100ns \qquad \text{Equation 4.3}$$

The pulse widths for the read and write signals are 200 ns when the 8051 is operating at 20MHz. When operation is slowed down to 7.3728, the t_{CLCL} drops to 136 ns, yielding a t_{RLDV} of 513ns and a read/write pulse width of 716 ns. The RAD hard memory components have access times of 35 ns or less, allowing operation of this design at the 8051 maximum data rate.

The 8255 requires a read pulse width of 250 ns and has a 200 ns maximum requirement for data valid from read asserted. On writes, the 8255 requires only 100 ns, which falls well within the maximum speed of this design. Taking these 8255 read and write constraints into consideration, if only output functions are being utilized, a 20MHz clock may be used. However, if input from the 8255 is desired, the speed must be slowed down to 17 MHz.

PIN	FUNCTION	PIN	FUNCTION
1	8255 #2 PORT A I/0 0	21	T/S DATA IN 17
2	I/O 1	22	T/S DATA IN 18
3	I/O 2	23	T/S DATA IN 19
4	I/O 3	24	T/S DATA IN 20
5	I/O 4	25	T/S DATA IN 21
6	I/O 5	26	T/S DATA IN 22
7	I/O 6	27	T/S DATA IN 23
8	I/O 7	28	T/S DATA IN 24
9	8255 #2 PORT B I/O 0	29	T/S DATA IN 25
10	I/O 1	30	T/S DATA IN 26
11	I/O 2	31	T/S DATA IN 27
12	I/O 3	32	T/S DATA IN 28
13	I/O 4	33	T/S DATA IN 29
14	I/O 5	34	T/S DATA IN 30
15	I/O 6	35	T/S DATA IN 31
16	I/O 7	36	T/S DATA IN 32
17	8255 #2 PORT C I/O 4	37	
18	I/O 5	38	
19	I/O 6	39	
20	I/O 7	40	

Table 6: Connector 3

PIN	FUNCTION	PIN	FUNCTION
1	8255 #3 PORT A I/0 0	21	8255 #4 PORT A I/0 0
2	I/O 1	22	I/O 1
3	I/O 2	23	I/O 2
4	I/O 3	24	I/O 3
5	I/O 4	25	I/O 4
6	I/O 5	26	I/O 5
7	I/O 6	27	I/O 6
8	I/O 7	28	I/O 7
9	8255 #3 PORT B I/O 0	29	8255 #4 PORT B I/O 0
10	I/O 1	30	I/O 1
11	I/O 2	31	I/O 2
12	I/O 3	32	I/O 3
13	I/O 4	33	I/O 4
14	I/O 5	34	I/O 5
15	I/O 6	35	I/O 6
16	I/O 7	36	I/O 7
17	8255 #3 PORT C I/O 4	37	8255 #4 PORT C I/O 4
18	I/O 5	38	I/O 5
19	I/O 6	39	I/O 6
20	I/O 7	40	I/O 7

Table 7: Connector 4

K. COMPLETE DESIGN DIAGRAM

Figure 13 shows the complete layout of this board design. Decoupling capacitors are omitted, as well as the specific connector layout, which is available elsewhere in this document.

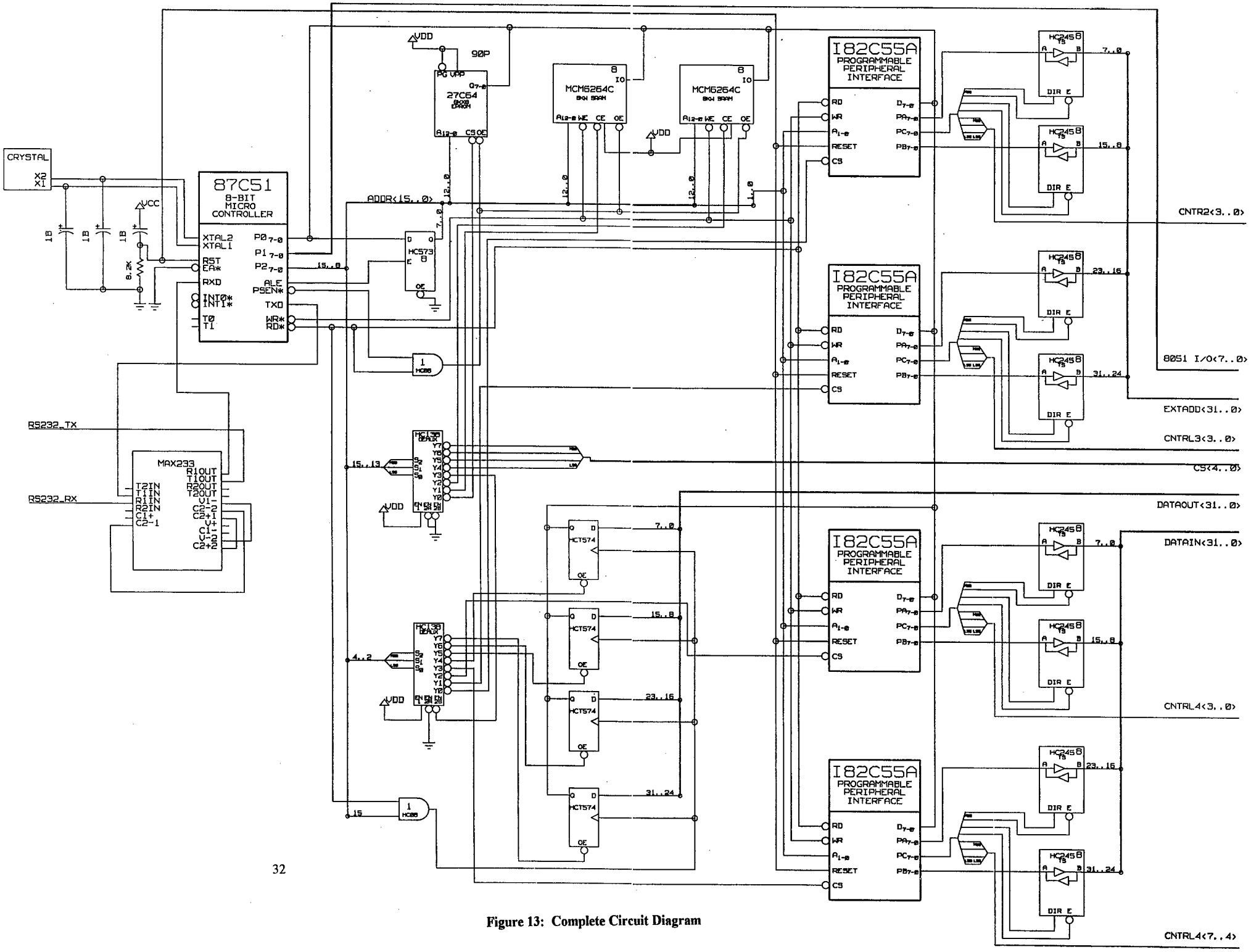

Figure 13: Complete Circuit Diagram

V. PROGRAMMING

A. OVERVIEW

In order to use the test hardware to test IC devices, a test program must be written, the board configured, and a test fixture created. This chapter will deal with all of these requirements, as well as describing some of the specific tests that the hardware will run.

B. BOARD CONFIGURATION

This process consists of determining which parts of the board are to be utilized and then writing a configuration routine to set up the appropriate parameters. This initialization may be run separately or incorporated as part of the actual test program. The simplest initialization program is actually no program at all. When the board is initialized, the 8255 ports are configured as inputs and the 8051 bus is fully accessible. Any simple memory device with 8 data bits and up to 32K of address space can be connected directly to the microcontroller bus (available on connector 1) with no additional setup requirements.

The 8255 will operate in one of three basic modes, byte input, byte output, and bit-set mode. As mentioned before, for byte input mode, the data simply needs to be read from the appropriate address, as shown below in Table 8.

MEMORY LOCATION	USE	MEMORY LOCATION	USE
6000H	PORT A 8255 #1	600AH	PORT C 8255 #3
6001H	PORT B 8255 #1	600BH	8255 #3 CONTROL WORD
6002H	PORT C 8255 #1	600CH	PORT A 8255 #4
6003H	8255 #1 CONTROL WORD	600DH	PORT B 8255 #4
6004H	PORT A 8255 #2	600EH	PORT C 8255 #4
6005H	PORT B 8255 #2	600FH	8255 #4 CONTROL WORD
6006H	PORT C 8255 #2	6010H	LATCHED BYTE 0
6007H	8255 #2 CONTROL WORD	6014H	LATCHED BYTE 1
6008H	PORT A 8255 #3	6018H	LATCHED BYTE 2
6009H	PORT B 8255 #3	601CH	LATCHED BYTE 3

Table 8: Memory Map

To set up the I/O mode, the appropriate byte must be written to the 8255 control word. The most common I/O type, mode 0, performs basic byte input and output. The layout of the control word is shown in Figure 14. To set up port A as output, bit 7 must be set, bits 5 and 6 need to be 00 for Mode 0, and bit 4 needs to be 0 for output. Hence, to set up the #1 8255 port A for output mode, write 1000xxxxB (here x is don't care, and B is binary) to address 6003H. Then, it is simply a matter of writing the data byte that is to be put on port A to address 6000H. Port C is broken into an upper half and a lower half and each half can be independently set for input or output. To set up the lower half of port C for output, control bit 7 must be set, bit 2 should be cleared, and bit 0 should be cleared. Hence, a control word of 1xxxx0x0B should be written to the control register. Of course, it should be noted that if ports A and C are to both be used, the control words must be combined yielding a control word of 1000x0x0B.

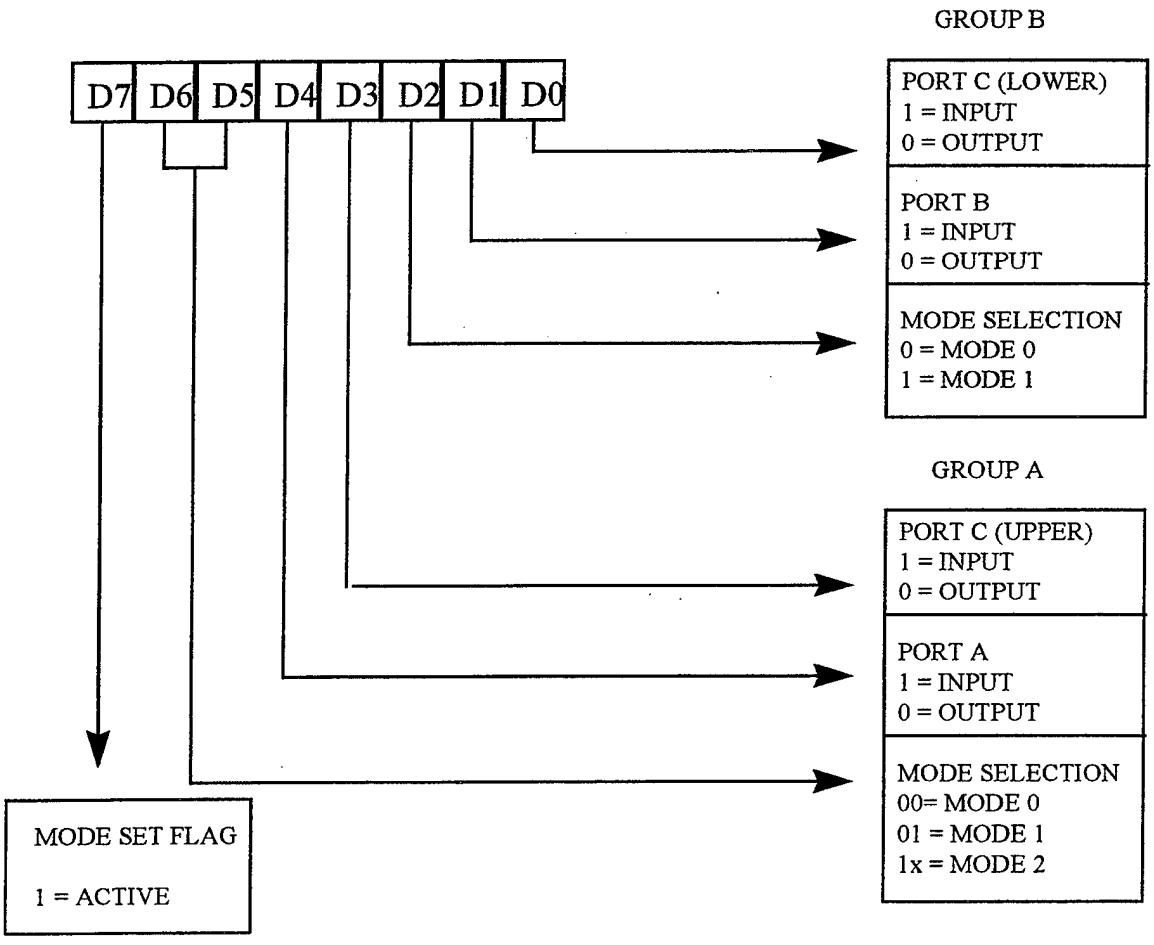

Figure 14: 8255 Control Word

C. ENABLING TRANCEIVERS

Once the modes of the 8255 ports are configured, the bus transceivers must be enabled and configured for the proper directions. Table 9 shows which bits of the upper C port control which transceiver functions

Port C bit	Function
bit 7	Port A direction (0 = input, 1 = output
bit 6	Port A enable (0 = enabled)
bit 5	Port B direction (0 = input, 1=output)
bit 4	Port B enable (0 = enabled)

Table 9: Transceiver Enables

To set up Port A as output, bit 7 must be set and bit 6 must be cleared, yielding a control word of 10xxxxxx. To set up Port B as input, bits 4 and 5 must be cleared. The combined control word for output on Port A and input on Port B is 1000xxxxB. It should be noted the lower half of Port C is available as a 4-bit input or output port.

D. PROGRAMMING

In order to actually perform tests, a program must be written. This program is written in 8051 assembly language and must be debugged, compiled, and loaded as with any assembly language program. The assembler used for this work is a shareware version called A51. Once the program is written, it must be loaded onto the test board by either RAM download or PROM program. The actual 'operating system' of this board is a monitor program called PAULMON, which was developed at Oregon State University. On top of this monitor is a front-end that will run any of the test routines written as part of this research, as well as provide instruction on how to download additional programs. The monitor occupies address space from 0000H-0FFFH in its basic form and occupies through 1FFFH if disassembler and debugger options are used. The monitor provides functions for serial I/O as well as memory editing, program downloading, and memory dumping. A listing of built-in functions is shown in Appendix A.

The easiest way to load a program is to download it via the RS-232 serial port and then run it from the monitor. For this method, address 2000H starts the RAM area. A complete description of the process is detailed below in the Vitesse section.

E. TEST DEVICE INTERFACE

Once the board is set up and the program is functioning, the device to be tested must be interfaced with the board. For each device to be tested, a separate test fixture must be built to interface with the test hardware connectors. For most applications, two, 40-conductor ribbon cables will carry the signals to the test fixture of the device under tested. Typically, only a socket and two 40-pin headers are required. This method was chosen for maximum flexibility, as there are so many package types and many different power configurations per package.

F. VITESSE

The setup for the Vitesse SRAM is very simple. It must be connected to the microcontroller bus, therefore requiring only connector 1. The layout of the IC is 8 address lines, 4 data in lines, 4 data out lines, and the usual read, write, and chip-select lines. Only the active-low enable line is used, therefore the active-high chip select line is tied high. The address lines are wired to the address 0-7 lines on connector 1, along with the read, write, and one of the chip-select lines (the 8000H line was used here). The only remaining lines are the data lines, of which it was decided to wire the inputs to data 0-3 and the outputs to data 4-7.

The program is relatively straight forward, simply write a fixed value to addresses 8000H-80FFH and then read the values back. The only small glitch in this procedure is that the data read must be ANDed with F0H before a comparison is made. The assembly language follows:

```
; Written by Duane Amsler as part of masters thesis

; the following program writes a value of 55H to memory locations 8000H-80FFH and then
; reads back the data in those locations. The read data is then masked with F0H to disregard
; the lower 4 bits, as this program is designed to test a 4-bit memory device


; initial assignments to allow output of memory locations and ASCII data

.equ    Cout, 0x0030      ;Send Acc to serial port

.equ    pHex16, 0x0036    ;Print Hex value of DPTR
```

```
.ORG H'2000                ; start this program within the RAM space at 2000H

        mov dptr, #h'3000  ; set up test address to start at 8000H
        mov a,h'55         : us a value of 55H (01010101B) as a test pattern
loopd1: movx @dptr,a       ; move accumulator to memory at data pointer (dptr)
        inc dpt            ; increment the data pointer
        mov r7,dpl         ; move the lower half of the data pointer to register 7
        cjne r7,#0,loopd1  ; if the data pointer lower byte is not 0, continue

        ret                ; return

.ORG H'2100                ; start this program within the RAM space at 2100H

read:  mov dptr,#h'8000    ; start reading data from address 8000H
loopr1: movx a,@dptr       ; load the data at data pointer to the accumulator
        anl a,#h'F0        ; mask out the lower 4 bits
        cjne a,#h'05,error ; if the value is x5, continue, else jump to error
        inc dptr           ; increment the data pointer
        mov r7,dpl         ;move the lower data pointer byte to register 7
        cjne r7,#0,loopr1  ; if lower data pointer is 00 exit, else continue
        ret                ; return to the calling program


error: lcall cout          : if error, call cout (will print the accumulator value,
                           : which will not be x5H if error was called)
        mov a,#' '         ; load accumulator with ASCII value for space
        lcall cout         ; output the space in the accumulator
        lcall phex16       ; output the value of the data pointer ( the location where
                           ; the error occurred
        mov a,#h'55        ; move 55 into the accumulator
        movx @dptr,a       ; store 55 in the location where the error occurred
        ajmp loopr1        ; jump back to the check loop
```

The above program was tested in RAM at location 3000H. The first routine was run from the monitor and then values written were verified by a memory dump. After the correct data was verified, a memory location was edited to a different value and the second routine was run. The value was correctly detected, corrected, and output to the laptop via the serial port.

VI. CONCLUSIONS

A. DESIGN CONCLUSIONS

The overall design of the test hardware was fairly straight forward, although designing to test up to a 32-bit device with an 8-bit microcontroller was rather challenging. The basic memory layout is widely used in applications notes and required some modification. The latching and shifting circuitry is original and may not be the most optimal solution, which will allow for future scrutiny and possible optimization of this work. It may be possible to program the 8255s to latch and hold. However, this will require additional configuration lines, which may be implemented as DIP switches, outputs from the 8051, or 8255 outputs.

B. BOARD FABRICATION

The board design is laid out in the CADENCE design tool CONCEPT, and can be converted into a GERBER file for fabrication. This will provide a reliable board that is much more elegant than the prototype board that was wire-wrapped.

C. COMPONENT COST

The RAD hard parts are very expensive and will require a fair amount of funding to purchase. The United Technologies VLSI parts range from $1500-$1900, while their commercial counterparts range from $3-$20. The United Technologies MSI RAD hard logic devices are all $166, as opposed to the commercial MSI component costs of less than a dollar.

D. PROGRAMMING & TESTING

The initial attempt to test a Vitesse SRAM caused the microcontroller bus to fail. This may be the result of heavy loading of the bus by the part, or a faulty part. The next test will be to isolate the SRAM from the microcontroller bus and perform the tests under manual control of the 8255s. This will require the control lines be simulated with the bit set and clear capabilities of port C of the 8255. This work is ongoing.

E. FOLLOW-ON WORK

There are a few areas that may allow significant follow-on work. The most obvious is actually testing the LT GaAs experimental chips, as well as this board, in a radiation environment.

1. Produce Professional PC Board

To improve upon system reliability and robustness, a commercially-produced PC board should be considered to both increase capabilities to 32 bits, as well as provide an aesthetically pleasing package for transport to radiation test sites.

2. Use RAD Hard components

The intent of this design was to create a unit capable of testing ICs in a radiation environment. In its current configuration (with commercial parts), lead bricks must be set up around this board to shield it from radiation. This method will work, but is far from the optimal solution.

3. ECC on Serial Link

The serial link currently uses a MAX233, which has no RAD hard counterparts. The 1488/1489 family also has no RAD hard counterpart. Because of this, some sort of error correcting code should be used on the RS-232 serial link. This will ensure proper data is obtained on tests. Something simple, such as a parity bit, possibly with check summing and retransmission, could be used. Further research is warranted.

4. Use of a C Compiler

To aid in the development of test programs, a high-level language could be used. Although assembly language is still useful, the use of C will aid in increasing program complexity and program development speed.

5. Creating a Script Language

Instead of another high-level language such as C, a scripting language could be developed to create an intuitive method for programming tests.

F. SUMMARY

This overall design was a valuable learning tool and should provide some functionality and utility in the future. This research should serve as a good starting point for improved designs, as well as an example of good, general-purpose test hardware.

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1. Christopher S. Mooney, "Design of a Satellite Based Microelectronic Radiation Testing Experiment," Masters Thesis, Naval Postgraduate School Thesis, Monterey, CA, March, 1996.
2. Wertz and Larson, *Space Mission Analysis and Design*, Kluwer Academic Publishers, Norwell, MA, 1991.
3. Todd R. Weatherford, Paul W. Marshall, Cheryl Dale, Andrew Peczalski, S. Baier, Dale McMorrow, Mark Twigg, and Arthur B. Campbell, "Soft Error Immune LT GaAs ICs", paper to be presented at the 18th Annual IEEE Gallium Arsenide Integrated Circuits Conference, Orlando, FL, November 3 - 6, 1996.
4. Greg Goodhue, "RAM loader program for 80C51 applications," Phillips Semiconductors Application Note AN440, June, 1993.
5. "UT69RH051 Address/Data Demultiplexer," UTMC Application Note, January, 1996.

APPENDIX A. PAULMON DOCUMENTAION

The following is the documentation file for PAULMON, and although it is a bit rough, it does contain a wealth of valuable information.

Introduction:

The PAULMON debugger is my attempt to make a user-friendly 8051 debugger, with enough on-line information that it should be unnecessary to read this doc file. PAULMOM is targeted for use by the microprocessor design course at Oregon State, but may be used by anyone (who can figure it out) for projects ranging from research to commercial products. PAULMON is free and may not be distributed for profit whatsoever.

Since I don't expect Prof's or TA's at OSU to make students aware of this documentation nor to provide it nor do I expect students to read much of it, I wrote PAULMON to be very simple and to provide lots of on-line clues about that it can do and how to go about it. I hope that you find PAULMON to be useful and easy to use. Good Luck.

-Paul Stoffregen

(paul@ece.orst.edu)

DISCLAIMER: This is free software. As far as warranty is concerned, you get exactly what you pay for! I have tried to make this code as good as possible during the four weeks I worked on it, but nobody is perfect and portions (the single step in particular) were never well tested. USE AT YOUR OWN RISK. The assembly source is provided in case there's something you don't like.

ADDITIONAL DISCLAIMER: This doc file has lots of tyopes and other errorss, and I really don't care. PAULMON was written to be easy enough that this file ought to be unnecessary, but people ask for it nonetheless, usually before they even try to use the thing.

What You Will Need to use it:

PAULMON is 8051 assembly code which is intended to be burned into a 2764 EPROM, though a pair of 2732's could be used or a bigger rom can be used with the rest being empty or filled with other code. The EPROM with PAULMON should be addressed so that it is read from 0000 to 1FFF with the 8051's EA pin wired to make it read all code from external memory. PAULMON uses the built in UART in the 8051 to communicate with the user. Typically, a PC computer is used with a terminal program, an 8051 assembler, and a text editor to form a simple, low cost 8051 development system with PAULMON. A serial line receiver and driver should be used (the MAX232 is a good choice, IMHO) to interface the 8051 to the PC's serial port. Only TxD, RxD and ground are used (no handshaking) and PAULMON adapts to use whatever baud rate the computer is using (if it can with the crystal you select, see below)

PAULMON is intended to be used with RAM as well, and the default location for the beginning of the RAM is 2000 (hex), right after the EPROM, though the RAM can be used anywhere in the

range of 2000 - FFFF. The read enable signal to the RAM should be the logical OR of the RD and PSEN signals, so that read attempts to external code memory or program memory spaces will read from the RAM. (use an AND gate to do the logical OR of these signals, since they are active low!) Obviously the write enable of the RAM should be connected to the WR pin of the 8051.

Having a RAM connected in this way will allow the download command in PAULMON to write your program into the RAM (writing into the external data memory space). Then you can run your program, since read attempts from the external program memory space will read from the RAM chip.

How to get is set up:

Design and build your 8051 board. All that is really required is the 8051, an EPROM, a latch (74xx373), some sort of address decoding to enable the EPROM for memory access between 0000-1FFF, and a line receiver to convert the high voltage RS232 to a TTL (or CMOS) compatible signal (or else you'll toast the 8051 before it even has a chance).

To really use PAULMON, a RAM is required as well as the AND gate to allow both program and data read cycles to read the RAM memory, and a reset button to easily get back to PAULMON when your program crashes.

With just the minimal setup, set the computer's baud rate to something slow (like 1200 bps) and power up the board. Press Enter (Return) and hopefully you'll see a screenful of text from PAULMON. PAULMON does not send line feed characters, so the terminal emulator software must be configured to translate CR -> CR/LF. (PAULMON ignores LF characters is receives.) If the entire message ends up on one line, then the terminal is not translating CR -> CR/LF. After it works, you can try increasing the baud rate and COLD-BOOTING (you must turn the power off, taking the reset line high will not make PAULMON look for the new baud rate... or change the bytes where it stores the old baud rate... see the code if you're interested) If the minimal system shows no signs of life, it's time to check the wiring, usually starting by making sure you didn't swap the TxD and RxD lines.

The Automatic Baud Rate detection:

This code was borrowed from MDP/51 by Kei-Yong Khoo. It is run immediatly after a system reset. It waits for a <RETURN> character, and uses it to calculate the timer #1 reload value. Some modifications have been made to Khoo's code. It requires only one character. It also stores the reload value in four memory locations in internal ram (78H, 79H, 7AH, and 7BH). These four locations are unlikely to be changed during a user program's execution or while the debugger is running. When another reset occurs (without removing the power) the program looks at those four locations. If all four agree, then it uses that reload value and does not require another keypress. It is interesting to note that occasionally, with cystal values which produce exact reload values (such an 7.3728 MHz), the baud rate detection routine may not correctly calculate the reload value. Garbage will get printed all over the screen. If this happens, just switch off the power and try again. The advantage of crystals such as the 7.3728 Mhz is that they allow transmission at speeds of 9600 and 19200 baud! It is highly reccomended that you use the highest possible baud rate with this debugger, as is tends to print quite a bit of text to the screen.

On-line Help:

By typing '?' at the main menu, a help screen summarizing the available commands is printed. On-line help is also available regarding the single step run feature. This help is accessed by typing '?' just after using the 'R' command. While in the single step mode, a summary of commands is also available, again by typing '?'.

The <ESC> key:

The <ESC> key is supported extensively. It will abort all commands from any prompt. It will stop the list and hex dump commands in the middle of their printing. It will also interrupt the printing of text to the screen! This is useful at slow baud rates, since a full screen of text can take quite a while to print at 300 baud.

The Download Program command (type 'D')

This allows you to send the object code from the assembler to the external ram. The object file must be a standard Intel Hex Format file, such as the .OBJ file created by the Psuedo- Assembler, by Psuedo-Corp. The file must be sent as an ASCII transfer. The protocal such as XMODEM is used. Pressing the <ESC> key at any time will abort the transfer. Please note that most communications programs use the <ESC> key to abort their transfer. In this is the case, the first <ESC> will halt the terminal, pressing it again will abort the recieve at the 8051/31. Unlike some other debuggers, PAULMON will recognize the <ESC> key anywhere in the middle of the incoming data, not just at the beginning of a line.

The Run Program command (type 'R')

The run command allows you to execute your program. Two types of run are supported, Normal and Single-Step. The single step mode is explained later, as it is fairly complex. During a normal run, the quiviliant of an LCALL to your code is given. During the execution of your program, the debugger obviously has no control of the system, unless of course your program calls one of the subroutines offered by the degugger in the jump table at location 0030H. After specifying which run mode you need, the location of your program is prompted, with the current memory pointer value as the default choice. As is the case at all prompts, pressing the <ESC> key will abort the run command. It is interesting to note that the run command leaves timer #1 in auto-baud rate generation mode. If serial communication is desired at the same baud rate as that used for the debugger, timer #1 need not be given a new reload value. It is recommended that the character input and output routines from the debugger be used via the jump table.

The New Memory Location command (type 'N')

The debugger operates with a pointer to the data memory with which you are working. This pointer is used by the list and hex dump command. It is also the default run location. The pointer is incremented as memory is viewed or modified. Just type 'N' to change it.

The List command (type 'L')

This debugger gives you the ability to list your program's code directly from the computer's memory. All the 8051/31 mnemunonics are supports, as well as the names of the special function registers. Bit addressable locations are displayed using the standard syntax (e.g. PWS.2 or 20.5), but individual bit location names are not supported (e.g. SCON.0 will print in place of RI). Obviously, the original labels used in the source code cannot be printed, instead the memory locations are displayed. Other special Intel assembly formats, such as $ and CALL are not

supported. However, the list command can provide a reassuring look at the program directly from the memory.

The Hex Dump command (type 'H')

By typing 'H', the next 256 bytes of ram are dumped to the screen in hex and ascii. The <ESC> key may be pressed to abort the printout.

The Edit command (type 'E')

This command allows you to change the values of memory locations in the external ram. Each location's old value is shown. If <ESC> is pressed, the current location's value is not changed.

The Jump Table:

Desipte the use of the word "jump", the user must LCALL to these locations! The individual locations contain jumps to the subroutines, which all terminate with a RET. The table provides the user with a memory location to call to that WILL NOT CHANGE if the debugger is reassembled. The routines available are:

0030: Cout -Sends the byte in Acc to the serial port.

0032: Cin -Waits for a character from the serial port, returned in Acc.

0034: pHex -Prints the two digit hex value in Acc to the serial port.

0036: pHex16 -Prints the four digit hex value in DPTR to the serial port.

0038: pString -Prints the string in code memory pointed to by DPTR to the serial port. The string must terminate with 00H or a high bit set

003A: gHex -Gets a two digit hex value from the serial port, returned in Acc

003C: gHex16 Gets a four digit hex value from the serial port, returned in DPTR

003E: Esc -Checks to see if the <ESC> key is waiting in SBUF. Clears the buffer if it is, and returns with the carry set. Otherwise, leaves SBUF untouched, and returns with C=0.

0040: Upper -Converts character in Acc to uppercase if it is lowercase

0042: Init -Automatic baud rate detection.

The memory location can be placed directly in your code, or an EQU can be used to make your code more readable. For example:

```
Program:.EQU   gHex16, 003AH     ;this make the code nice
        MOV    DPTR, #StrLoc     ;load DPTR
        LCALL  gHex16            ;print the DPTR
        MOV    A,#13
        LCALL  0030H             ;print a <RET>
        LCALL  0038H             ;print the string
```

RET StrLoc: .DB "This is my String.", 0

Most of these routines leave the registers unchanged, however, it is a good idea to consult the source code just to be sure... In particular, the phex routine DESTROYS the contents of Acc, so beware. (this has cause some people some grief, who had assumed the phex would leave Acc unchanged. If you want it unchanged, the original .ASM file is provided for you to modify) The

Single-Step Run:

[This part was never written, and the single step run code is somewhat buggy, primarily due to a lack of available beta testers... so docs were never written, but PAULMON ought to give you enough clues to figure it out if you try.]

APPENDIX B. 8051 PROGRAMMERS REFERENCE

PROGRAMMER'S GUIDE AND INSTRUCTION SET

Memory Organization

Program Memory

The 80C51 has separate address spaces for program and data memory. The Program memory can be up to 64k bytes long. The lower 4k can reside on-chip. Figure 1 shows a map of the 80C51 program memory.

The 80C51 can address up to 64k bytes of data memory to the chip. The MOVX instruction is used to access the external data memory.

The 80C51 has 128 bytes of on-chip RAM, plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @Ri). Figure 2 shows the Data Memory organization.

Direct and Indirect Address Area

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into three segments as listed below and shown in Figure 3.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers 0 through 7. Reset initializes the stack pointer to location 07H, and it is incremented once to start from location 08H, which is the first register (R0) of the second register bank. Thus, in order to use more than one register bank, the SP should be initialized to a different location of the RAM where it is not used for data storage (i.e., the higher part of the RAM).
2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). The bits can be referred to in two ways, both of which are acceptable by most assemblers. One way is to refer to their address (i.e., 0-7FH). The other way is with reference to bytes 20H to 2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 8-FH are the same as 21.0-21.7, and so on. Each of the 16 bytes in this segment can also be addressed as a byte.
3. Scratch Pad Area: 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

Figure 2 shows the different segments of the on-chip RAM.

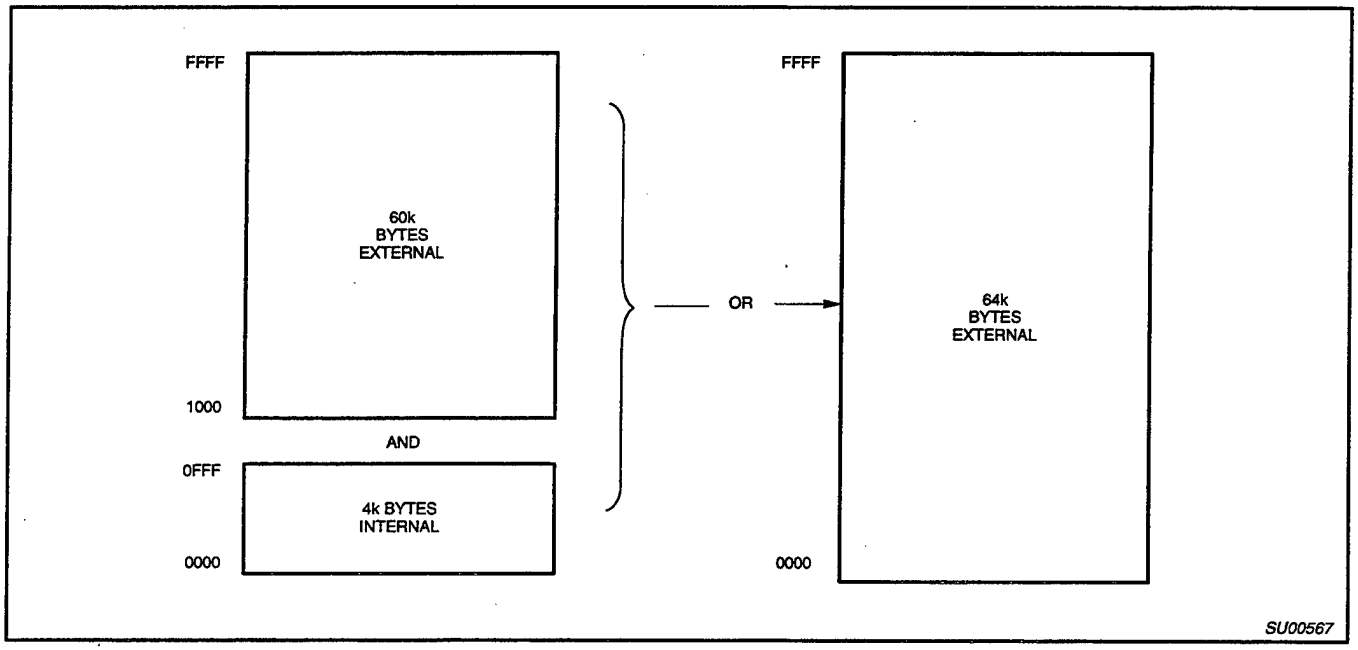


Figure 1. 80C51 Program Memory

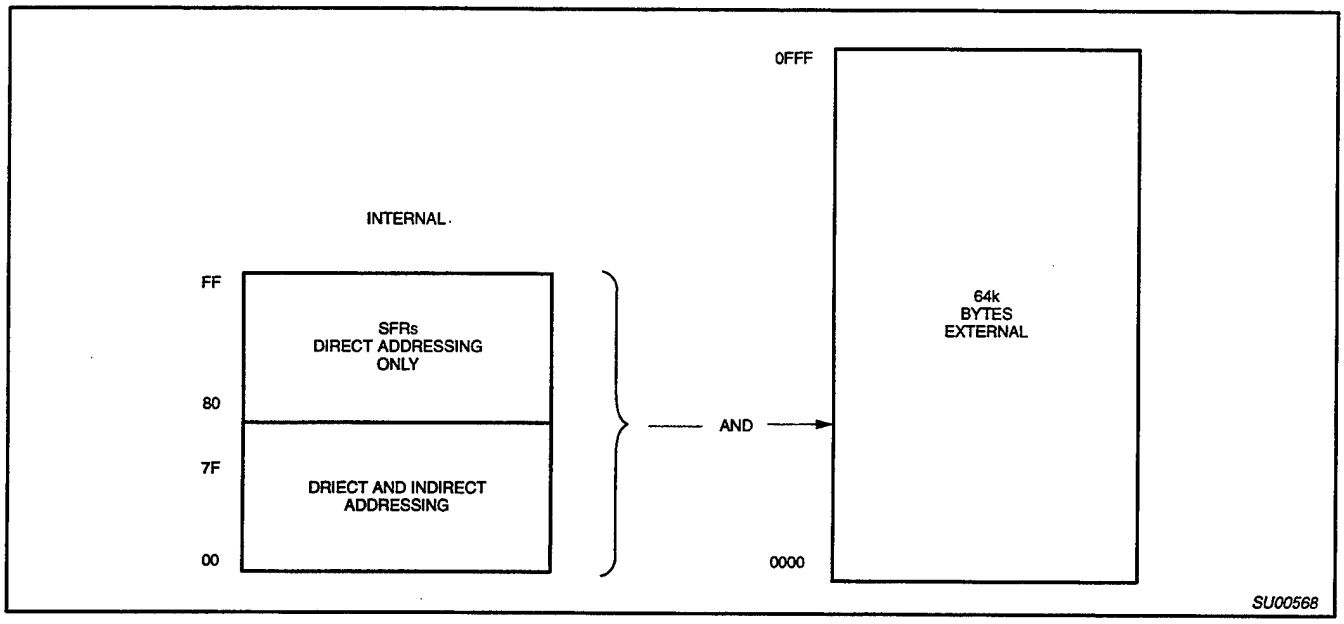


Figure 2. 80C51 Data Memory

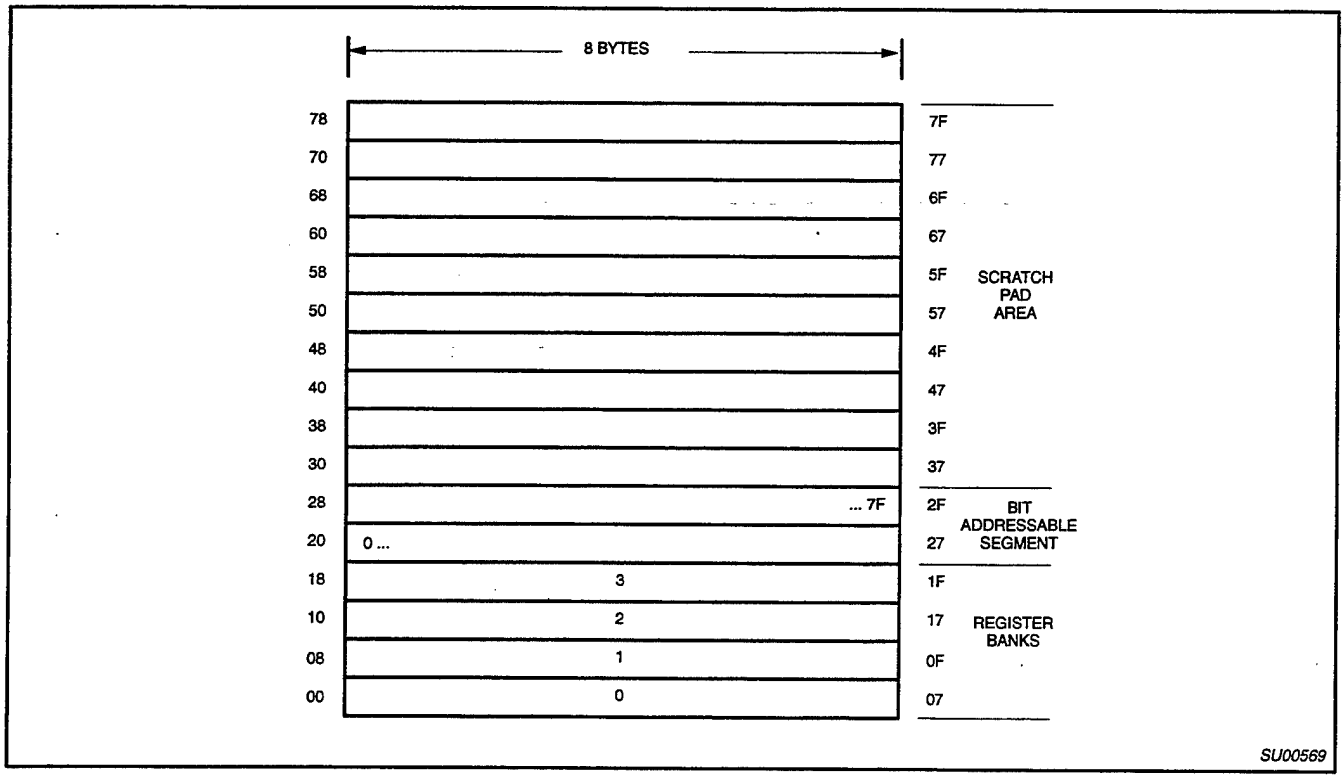


Figure 3. 128 Bytes of RAM Direct and Indirect Addressable

Table 1. 80C51 Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR	Data pointer (2 bytes)										
DPH	Data pointer high	83H									00H
DPL	Data pointer low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt enable	A8H	EA	–	–	ES	ET1	EX1	ET0	EX0	0x000000B
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt priority	B8H	–	–	–	PS	PT1	PX1	PT0	PX0	xx000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	A15	A14	A13	A12	A11	A10	A9	A8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	Rxd	FFH
PCON[1]	Power control	87H	SMOD	–	–	–	GF1	GF0	PD	IDL	0xxxxxxxB
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
SBUF	Serial data buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial controller	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
TH0	Timer high 0	8CH									00H
TH1	Timer high 1	8DH									00H
TL0	Timer low 0	8AH									00H
TL1	Timer low 1	8BH									00H
TMOD	Timer mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H

NOTES:
* Bit addressable
1. Bits GF1, GF0, PD, and IDL of the PCON register are not implemented on the NMOS 8051/8031.

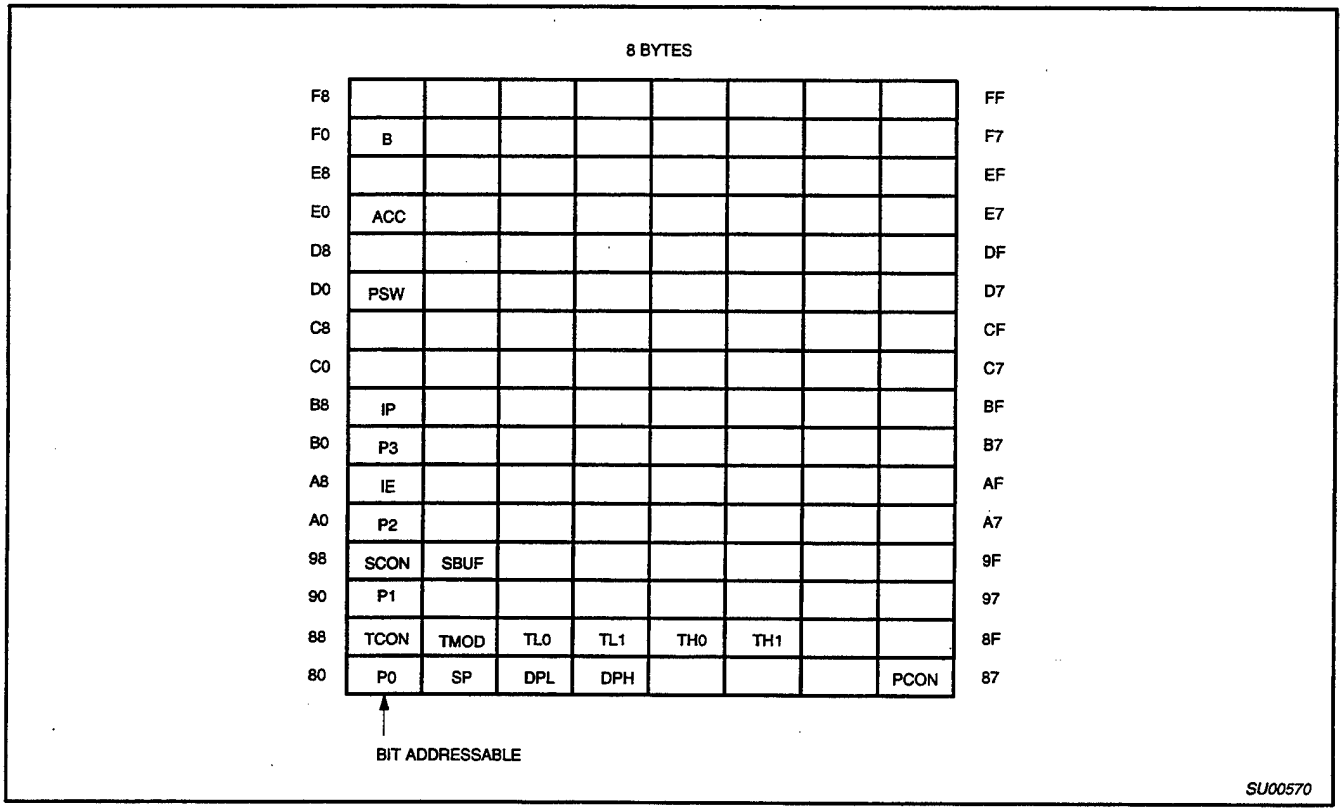


Figure 4. SFR Memory Map

Those SFRs that have their bits assigned for various functions are listed in this section. A brief description of each bit is provided for quick reference. For more detailed information refer to the Architecture Chapter of this book.

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
–	PSW.1	Usable as a general purpose flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bus in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

PCON: POWER CONTROL REGISTER. NOT BIT ADDRESSABLE.

SMOD	–	–	–	GF1	GF0	PD	IDL

SMOD Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD = 1, the baud rate is doubled when the Serial Port is used in modes 1, 2, or 3.

– Not implemented, reserved for future use.*

– Not implemented reserved for future use.*

– Not implemented reserved for future use.*

GF1 General purpose flag bit.

GF0 General purpose flag bit.

PD Power Down Bit. Setting this bit activates Power Down operation in the 80C51. (Available only in CMOS.)

IDL Idle mode bit. Setting this bit activates Idle Mode operation in the 80C51. (Available only in CMOS.)

If 1s are written to PD and IDL at the same time, PD takes precedence.

* User software should not write 1s to reserved bits. These bits may be used in future 8051 products to invoke new features.

INTERRUPTS:

To use any of the interrupts in the 80C51 Family, the following three steps must be taken.

1. **Set the EA (enable all) bit in the IE register to 1.**
2. **Set the corresponding individual interrupt enable bit in the IE register to 1.**
3. **Begin the interrupt service routine at the corresponding Vector Address of that interrupt. See Table below.**

INTERRUPT SOURCE	VECTOR ADDRESS
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI & TI	0023H

In addition, for external interrupts, pins INT0 and INT1 (P3.2 and P3.3) must be set to 1, and depending on whether the interrupt is to be level or transition activated, bits IT0 or IT1 in the TCON register may need to be set to 1.

ITx = 0 level activated

ITx = 1 transition activated

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserved for future use.*
—	IE.5	Not implemented, reserved for future use.*
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External Interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

* User software should not write 1s to reserved bits. These bits may be used in future 80C51 products to invoke new features.

ASSIGNING HIGHER PRIORITY TO ONE OR MORE INTERRUPTS:

In order to assign higher priority to an interrupt the corresponding bit in the IP register must be set to 1.

Remember that while an interrupt service is in progress, it cannot be interrupted by a lower or same level interrupt.

PRIORITY WITHIN LEVEL:

Priority within level is only to resolve simultaneous requests of the same priority level.

From high to low, interrupt sources are listed below:

IE0
TF0
IE1
TF1
RI or TI

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

–	–	–	PS	PT1	PX1	PT0	PX0

–	IP.7	Not implemented, reserved for future use.*
–	IP.6	Not implemented, reserved for future use.*
–	IP.5	Not implemented, reserved for future use.*
PS	IP.4	Defines the Serial Port interrupt priority level.
PT1	IP.3	Defines the Timer 1 interrupt priority level.
PX1	IP.2	Defines External Interrupt 1 priority level.
PT0	IP.1	Defines the Timer 0 interrupt priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level.

* User software should not write 1s to reserved bits. These bits may be used in future 80C51 products to invoke new features.

TCON: TIMER/COUNTER CONTROL REGISTER. BIT ADDRESSABLE.

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1	TCON.7	Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.
TR1	TCON.6	Timer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF.
TF0	TCON.5	Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as processor vectors to the service routine.
TR0	TCON.4	Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF.
IE1	TCON.3	External Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by hardware when interrupt is processed.
IT1	TCON.2	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.
IE0	TCON.1	External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed.
IT0	TCON.0	Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

TMOD: TIMER/COUNTER MODE CONTROL REGISTER. NOT BIT ADDRESSABLE.

GATE	C/T	M1	M0	GATE	C/T	M1	M0
		Timer 1				Timer 0	

GATE	When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx will run only while INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control).
C/T	Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).
M1	Mode selector bit. (NOTE 1)
M0	Mode selector bit. (NOTE 1)

NOTE 1:

M1	M0		Operating Mode
0	0	0	13-bit Timer (8048 compatible)
0	1	1	16-bit Timer/Counter
1	0	2	8-bit Auto-Reload Timer/Counter
1	1	3	(Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standart Timer 0 control bits. TH0 is an8-bit Timer and is controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

TIMER SET-UP

Tables 2 through 5 give some values for TMOD which can be used to set up Timer 0 in different modes.

It is assumed that only one timer is being used at a time. If it is desired to run Timers 0 and 1 simultaneously, in any mode, the value in TMOD for Timer 0 must be ORed with the value shown for Timer 1 (Tables 5 and 6).

For example, if it is desired to run Timer 0 in mode 1 GATE (external control), and Timer 1 in mode 2 COUNTER, then the value that must be loaded into TMOD is 69H (09H from Table 2 ORed with 60H from Table 5).

Moreover, it is assumed that the user, at this point, is not ready to turn the timers on and will do that at a different point in the program by setting bit TRx (in TCON) to 1.

TIMER/COUNTER 0

Table 2. As a Timer:

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	00H	08H
1	16-bit Timer	01H	09H
2	8-bit Auto-Reload	02H	0AH
3	Two 8-bit Timers	03H	0BH

Table 3. As a Counter:

MODE	COUNTER 0 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	04H	0CH
1	16-bit Timer	05H	0DH
2	8-bit Auto-Reload	06H	0EH
3	One 8-bit Counter	07H	0FH

NOTES:
1. The timer is turned ON/OFF by setting/clearing bit TR0 in the software.
2. The Timer is turned ON/OFF by the 1-to-0 transition on $\overline{INT0}$ (P3.2) when TR0 = 1 (hardware control).

TIMER/COUNTER 1

Table 4. As a Timer:

MODE	TIMER 1 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	00H	80H
1	16-bit Timer	10H	90H
2	8-bit Auto-Reload	20H	A0H
3	Does not run	30H	B0H

Table 5. As a Counter:

MODE	COUNTER 1 FUNCTION	TMOD	
		INTERNAL CONTROL (NOTE 1)	EXTERNAL CONTROL (NOTE 2)
0	13-bit Timer	40H	C0H
1	16-bit Timer	50H	D0H
2	8-bit Auto-Reload	60H	E0H
3	Not available	–	–

NOTES:
1. The timer is turned ON/OFF by setting/clearing bit TR1 in the software.
2. The Timer is turned ON/OFF by the 1-to-0 transition on $\overline{INT1}$ (P3.2) when TR1 = 1 (hardware control).

SCON: SERIAL PORT CONTROL REGISTER. BIT ADDRESSABLE.

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0	SCON.7	Serial Port mode specifier. (NOTE 1)
SM1	SCON.6	Serial Port mode specifier. (NOTE 1)
SM2	SCON.5	Enables the multiprocessor communication feature in modes 2 & 3. In mode 2 or 3, if SM2 is set to 1 then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1 then RI will not be activated if a valid stop bit was not received. In mode 0, SM2 should be 0. (See Table 6.)
REN	SCON.4	Set/Cleared by software to Enable/Disable reception.
TB8	SCON.3	The 9th bit that will be transmitted in modes 2 & 3. Set/Cleared by software.
RB8	SCON.2	In modes 2 & 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	SCON.1	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes. Must be cleared by software.
RI	SCON.0	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes (except see SM2). Must be cleared by software.

NOTE 1:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift Register	$F_{OSC.}/12$
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	$F_{OSC.}/64$ or $F_{OSC.}/32$
1	1	3	9-bit UART	Variable

SERIAL PORT SET-UP:

Table 6.

MODE	SCON	SM2 VARIATION
0 1 2 3	10H 50H 90H D0H	Single Processor Environment (SM2 = 0)
0 1 2 3	NA 70H B0H F0H	Multiprocessor Environment (SM2 = 1)

GENERATING BAUD RATES

Serial Port in Mode 0:

Mode 0 has a fixed baud rate which is 1/12 of the oscillator frequency. To run the serial port in this mode none of the Timer/Counters need to be set up. Only the SCON register needs to be defined.

$$\text{Baud Rate} = \frac{\text{Osc Freq}}{12}$$

Serial Port in Mode 1:

Mode 1 has a variable baud rate. The baud rate is generated by Timer 1.

USING TIMER/COUNTER 1 TO GENERATE BAUD RATES:

For this purpose, Timer 1 is used in mode 2 (Auto-Reload). Refer to Timer Setup section of this chapter.

$$\text{Baud Rate} = \frac{K}{32} \times \frac{\text{Osc Freq}}{12 \times [256 - (TH1)]}$$

If SMOD = 0, then K = 1.
If SMOD = 1, then K = 2 (SMOD is in the PCON register).

Most of the time the user knows the baud rate and needs to know the reload value for TH1.

$$TH1 = 256 - \frac{K \times \text{Osc Freq}}{384 \times \text{baud rate}}$$

TH1 must be an integer value. Rounding off TH1 to the nearest integer may not produce the desired baud rate. In this case, the user may have to choose another crystal frequency.

Since the PCON register is not bit addressable, one way to set the bit is logical ORing the PCON register (i.e., ORL PCON,#80H). The address of PCON is 87H.

SERIAL PORT IN MODE 2:

The baud rate is fixed in this mode and is 1/32 or 1/64 of the oscillator frequency, depending on the value of the SMOD bit in the PCON register.

In this mode none of the Timers are used and the clock comes from the internal phase 2 clock.

SMOD = 1, Baud Rate = 1/32 Osc Freq.

SMOD = 0, Baud Rate = 1/64 Osc Freq.

To set the SMOD bit: ORL PCON,#80H. The address of PCON is 87H.

SERIAL PORT IN MODE 3:

The baud rate in mode 3 is variable and sets up exactly the same as in mode 1.

80C51 FAMILY INSTRUCTION SET

Table 7. 80C51 Instruction Set Summary

Interrupt Response Time: Refer to Hardware Description Chapter.

Instructions that Affect Flag Settings[1]

Instruction	Flag			Instruction	Flag		
	C	OV	AC		C	OV	AC
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C,bit	X		
MUL	0	X		ANL C,/bit	X		
DIV	0	X		ORL C,bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C,bit	X		
RLC	X			CJNE	X		
SETB C	1						

[1]Note that operations on SFR byte address 208 or bit addresses 209-215 (i.e., the PSW or bits in the PSW) will also affect flag settings.

Notes on instruction set and addressing modes:

Rn	Register R7-R0 of the currently selected Register Bank.
direct	8-bit internal data location's address. This could be an Internal Data RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)].
@Ri	8-bit internal data RAM location (0-255) addressed indirectly through register R1 or R0.
#data	8-bit constant included in the instruction.
#data 16	16-bit constant included in the instruction
addr 16	16-bit destination address. Used by LCALL and LJMP. A branch can be anywhere within the 64k-byte Program Memory address space.
addr 11	11-bit destination address. Used by ACALL and AJMP. The branch will be within the same 2k-byte page of program memory as the first byte of the following instruction.
rel	Signed (two's complement) 8-bit offset byte. Used by SJMP and all conditional jumps. Range is –128 to +127 bytes relative to first byte of the following instruction.
bit	Direct Addressed bit in Internal Data RAM or Special Function Register.

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS				
ADD	A,Rn	Add register to Accumulator	1	12
ADD	A,direct	Add direct byte to Accumulator	2	12
ADD	A,@Ri	Add indirect RAM to Accumulator	1	12
ADD	A,#data	Add immediate data to Accumulator	2	12
ADDC	A,Rn	Add register to Accumulator with carry	1	12
ADDC	A,direct	Add direct byte to Accumulator with carry	2	12
ADDC	A,@Ri	Add indirect RAM to Accumulator with carry	1	12
ADDC	A,#data	Add immediate data to A_{CC} with carry	2	12
SUBB	A,Rn	Subtract Register from A_{CC} with borrow	1	12
SUBB	A,direct	Subtract direct byte from A_{CC} with borrow	2	12
SUBB	A,@Ri	Subtract indirect RAM from A_{CC} with borrow	1	12
SUBB	A,#data	Subtract immediate data from A_{CC} with borrow	2	12
INC	A	Increment Accumulator	1	12
INC	Rn	Increment register	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
ARITHMETIC OPERATIONS (Continued)				
INC	direct	Increment direct byte	2	12
INC	@Ri	Increment indirect RAM	1	12
DEC	A	Decrement Accumulator	1	12
DEC	Rn	Decrement Register	1	12
DEC	direct	Decrement direct byte	2	12
DEC	@Ri	Decrement indirect RAM	1	12
INC	DPTR	Increment Data Pointer	1	24
MUL	AB	Multiply A and B	1	48
DIV	AB	Divide A by B	1	48
DA	A	Decimal Adjust Accumulator	1	12
LOGICAL OPERATIONS				
ANL	A,Rn	AND Register to Accumulator	1	12
ANL	A,direct	AND direct byte to Accumulator	2	12
ANL	A,@Ri	AND indirect RAM to Accumulator	1	12
ANL	A,#data	AND immediate data to Accumulator	2	12
ANL	direct,A	AND Accumulator to direct byte	2	12
ANL	direct,#data	AND immediate data to direct byte	3	24
ORL	A,Rn	OR register to Accumulator	1	12
ORL	A,direct	OR direct byte to Accumulator	2	12
ORL	A,@Ri	OR indirect RAM to Accumulator	1	12
ORL	A,#data	OR immediate data to Accumulator	2	12
ORL	direct,A	OR Accumulator to direct byte	2	12
ORL	direct,#data	OR immediate data to direct byte	3	24
XRL	A,Rn	Exclusive-OR register to Accumulator	1	12
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	12
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	12
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	12
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	12
XRL	direct,#data	Exclusive-OR immediate data to direct byte	3	24
CLR	A	Clear Accumulator	1	12
CPL	A	Complement Accumulator	1	12
RL	A	Rotate Accumulator left	1	12
RLC	A	Rotate Accumulator left through the carry	1	12
RR	A	Rotate Accumulator right	1	12
RRC	A	Rotate Accumulator right through the carry	1	12
SWAP	A	Swap nibbles within the Accumulator	1	12
DATA TRANSFER				
MOV	A,Rn	Move register to Accumulator	1	12
MOV	A,direct	Move direct byte to Accumulator	2	12
MOV	A,@Ri	Move indirect RAM to Accumulator	1	12

Table 7. 80C51 Instruction Set Summary (Continued)

	MNEMONIC	DESCRIPTION	BYTE	OSCILLATOR PERIOD
DATA TRANSFER (Continued)				
MOV	A,#data	Move immediate data to Accumulator	2	12
MOV	Rn,A	Move Accumulator to register	1	12
MOV	Rn,direct	Move direct byte to register	2	24
MOV	RN,#data	Move immediate data to register	2	12
MOV	direct,A	Move Accumulator to direct byte	2	12
MOV	direct,Rn	Move register to direct byte	2	24
MOV	direct,direct	Move direct byte to direct	3	24
MOV	direct,@Ri	Move indirect RAM to direct byte	2	24
MOV	direct,#data	Move immediate data to direct byte	3	24
MOV	@Ri,A	Move Accumulator to indirect RAM	1	12
MOV	@Ri,direct	Move direct byte to indirect RAM	2	24
MOV	@Ri,#data	Move immediate data to indirect RAM	2	12
MOV	DPTR,#data16	Load Data Pointer with a 16-bit constant	3	24
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A_{CC}	1	24
MOVC	A,@A+PC	Move Code byte relative to PC to A_{CC}	1	24
MOVX	A,@Ri	Move external RAM (8-bit addr) to A_{CC}	1	24
MOVX	A,@DPTR	Move external RAM (16-bit addr) to A_{CC}	1	24
MOVX	A,@Ri,A	Move A_{CC} to external RAM (8-bit addr)	1	24
MOVX	@DPTR,A	Move A_{CC} to external RAM (16-bit addr)	1	24
PUSH	direct	Push direct byte onto stack	2	24
POP	direct	Pop direct byte from stack	2	24
XCH	A,Rn	Exchange register with Accumulator	1	12
XCH	A,direct	Exchange direct byte with Accumulator	2	12
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	12
XCHD	A,@Ri	Exchange low-order digit indirect RAM with A_{CC}	1	12
BOOLEAN VARIABLE MANIPULATION				
CLR	C	Clear carry	1	12
CLR	bit	Clear direct bit	2	12
SETB	C	Set carry	1	12
SETB	bit	Set direct bit	2	12
CPL	C	Complement carry	1	12
CPL	bit	Complement direct bit	2	12
ANL	C,bit	AND direct bit to carry	2	24
ANL	C,/bit	AND complement of direct bit to carry	2	24
ORL	C,bit	OR direct bit to carry	2	24
ORL	C,/bit	OR complement of direct bit to carry	2	24
MOV	C,bit	Move direct bit to carry	2	12
MOV	bit,C	Move carry to direct bit	2	24
JC	rel	Jump if carry is set	2	24
JNC	rel	Jump if carry not set	2	24

Table 7. 80C51 Instruction Set Summary (Continued)

MNEMONIC		DESCRIPTION	BYTE	OSCILLATOR PERIOD
BOOLEAN VARIABLE MANIPULATION (Continued)				
JB	rel	Jump if direct bit is set	3	24
JNB	rel	Jump if direct bit is not set	3	24
JBC	bit,rel	Jump if direct bit is set and clear bit	3	24
PROGRAM BRANCHING				
ACALL	addr11	Absolute subroutine call	2	24
LCALL	addr16	Long subroutine call	3	24
RET		Return from subroutine	1	24
RETI		Return from interrupt	1	24
AJMP	addr11	Absolute jump	2	24
LJMP	addr16	Long jump	3	24
SJMP	rel	Short jump (relative addr)	2	24
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	24
JZ	rel	Jump if Accumulator is zero	2	24
JNZ	rel	Jump if Accumulator is not zero	2	24
CJNE	A,direct,rel	Compare direct byte to A_{CC} and jump if not equal	3	24
CJNE	A,#data,rel	Compare immediate to A_{CC} and jump if not equal	3	24
CJNE	RN,#data,rel	Compare immediate to register and jump if not equal	3	24
CJNE	@Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	24
DJNZ	Rn,rel	Decrement register and jump if not zero	2	24
DJNZ	direct,rel	Decrement direct byte and jump if not zero	3	24
NOP		No operation	1	12

INSTRUCTION DEFINITIONS

ACALL addr11

Function: Absolute Call

Description: ACALL unconditionally calls a subroutine located at the indicated address. The instruction increments the PC twice to obtain the address of the following instruction, then pushes the 16-bit result onto the stack (low-order byte first) and increments the Stack Pointer twice. The destination address is obtained by successively concatenating the five high-order bits of the incremented PC, opcode bits 7-5, and the second byte of the instruction. The subroutine called must therefore start within the same 2k block of the program memory as the first byte of the instruction following ACALL. No flags are affected.

Example: Initially SP equals 07H. The label "SUBRTN" is at program memory location 0345 H. After executing the instruction,

ACALL SUBRTN

at location 0123H, SP will contain 09H, internal RAM locations 08H and 09H will contain 25H and 01H, respectively, and the PC will contain 0345H.

Bytes: 2

Cycles: 2

Encoding:

a10 a9 a8 1	0 0 0 1	a7 a6 a5 a4	a3 a2 a1 a0

Operation: ACALL
(PC) ← (PC) + 2
(SP) ← (SP) + 1
(SP) ← (PC_{7-0})
(SP) ← (SP) + 1
(SP) ← (PC_{15-8})
(PC_{10-0}) ← page address

ADD A,<src-byte>

Function: Add

Description: ADD adds the byte variable indicated to the Accumulator, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B). The instruction,

ADD A,R0

will leave 6DH (01101101B) in the Accumulator with the AC flag cleared and both the Carry flag and OV set to 1.

ADD A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	1 r r r

Operation: ADD

$(A) \leftarrow (A) + (R_n)$

ADD A,direct

Bytes: 2

Cycles: 1

Encoding:

0 0 1 0	0 1 0 1	direct address

Operation: ADD

(A) ← (A) + (direct)

ADD A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 1 0	0 1 1 i

Operation: ADD

$(A) \leftarrow (A) + ((R_i))$

ADD A,#data

Bytes: 2

Cycles: 1

Encoding:

0 0 1 0	0 1 0 0	immediate data

Operation: ADD

(A) ← (A) + #data

ADDC A,<src-byte>

Function: Add with Carry

Description: ADDC simultaneously adds the byte variable indicated, the carry flag and the Accumulator contents, leaving the result in the Accumulator. The carry and auxiliary-carry flags are set, respectively, if there is a carry-out from bit 7 or bit 3, and cleared otherwise. When adding unsigned integers, the carry flag indicates an overflow occurred.

OV is set if there is a carry-out of bit 6 but not out of bit 7, or a carry-out of bit 7 but not out of bit 6; otherwise OV is cleared. When adding signed integers, OV indicates a negative number produced as the sum of two positive operands, or a positive sum from two negative operands.

Four source operand addressing modes are allowed: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B) with the carry flag set. The instruction,

ADDC A,R0

will leave 6EH (01101110B) in the Accumulator with AC cleared and both the Carry flag and OV set to 1.

ADDC A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 1 1	1 r r r

Operation: ADDC
(A) ← (A) + (C) + (R_n)

ADDC A,direct

Bytes: 2

Cycles: 1

Encoding:

0 0 1 1	0 1 0 1	direct address

Operation: ADDC
(A) ← (A) + (C) + (direct)

ADDC A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 1 1	0 1 1 i

Operation: ADDC
(A) ← (A) + (C) + ((R_i))

ADDC A,#data

Bytes: 2

Cycles: 1

Encoding:

0 0 1 1	0 1 0 0	immediate data

Operation: ADDC
(A) ← (A) + (C) + #data

AJMP addr11

Function: Absolute Jump

Description: AJMP transfers program execution to the indicated address, which is formed at run-time by concatenating the high-order five bits of the PC (*after* incrementing the PC twice), opcode bits 7-5, and the second byte of the instruction. The destination must therefore be within the same 2k block of program memory as the first byte of the instruction following AJMP.

Example: The label "JMPADR" is at program memory location 0123H. The instruction,

AJMP JMPADR

is at location 0345H and will load the PC with 0123H.

Bytes: 2

Cycles: 2

Encoding:

a10 a9 a8 0	0 0 0 1	a7 a6 a5 a4	a3 a2 a1 a0

Operation: AJMP
(PC) ← (PC) + 2
($PC_{10\text{-}0}$) ← page address

ANL <dest-byte>,<src-byte>

Function: Logical-AND for byte variables

Description: ANL performs the bitwise logical-AND operation between the variables indicated and stores the results in the destination variable. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: If the Accumulator holds 0C3H (11000011B) and register 0 holds 55H (01010101B) then the instruction,

ANL A,R0

will leave 41H (01000001B) in the Accumulator.

When the destination is a directly addressed byte, this instruction will clear combinations of bits in any RAM location or hardware register. The mask byte determining the pattern of bits to be cleared would either be a constant contained in the instruction or a value computed in the Accumulator at run-time. The instruction,

ANL P1,#01110011B

will clear bits 7, 3, and 2 of output port 1.

ANL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 0 1	1 r r r

Operation: ANL
(A) ← (A) ∧ (R_n)

ANL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 1 0 1	direct address

Operation: ANL
(A) ← (A) ∧ (direct)

ANL A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 1 0 1	0 1 1 i

Operation: ANL
(A) ← (A) ∧ ((R_i))

ANL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 1 0 0	immediate data

Operation: ANL
(A) ← (A) ∧ #data

ANL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 0 1	0 0 1 0	direct address

Operation: ANL
(A) ←(direct) ∧ (A)

ANL direct,#data

Bytes: 3

Cycles: 2

Encoding:

0 1 0 1	0 0 1 1	direct address	immediate data

Operation: ANL
(direct) ←(direct) ∧ #data

ANL C,<src-bit>

Function: Logical-AND for bit variables

Description: If the Boolean value of the source bit is a logical 0 then clear the carry flag; otherwise leave the carry flag in its current state. A slash ("/") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, *but the source bit itself is not affected.* No other flags are affected.

Only direct addressing is allowed for the source operand.

Example: Set the carry flag if, and only if, P1.0 = 1, ACC.7 = 1, and OV = 0:

```
MOV     C,P1.0  ;LOAD CARRY WITH INPUT PIN STATE
ANL     C,ACC.7;AND CARRY WITH ACCUM. BIT 7
ANL     C,/OV   ;AND WITH INVERSE OF OVERFLOW FLAG
```

ANL C,bit

Bytes: 2

Cycles: 2

Encoding:

1 0 0 0	0 0 1 0	bit address

Operation: ANL

$(C) \leftarrow (C) \wedge (bit)$

ANL C,/bit

Bytes: 2

Cycles: 2

Encoding:

1 0 1 1	0 0 0 0	bit address

Operation: ANL

$(C) \leftarrow (C) \wedge \overline{(bit)}$

CJNE <dest-byte>,<src-byte>,rel

Function: Compare and Jump if Not Equal

Description: CJNE compares the magnitudes of the first two operands, and branches if their values are not equal. The branch destination is computed by adding the signed relative-displacement in the last instruction byte to the PC, after incrementing the PC to the start of the next instruction. The carry flag is set if the unsigned integer value of <dest-byte> is less than the unsigned integer value of <src-byte>; otherwise, the carry is cleared. Neither operand is affected.

The first two operands allow four addressing mode combinations: the Accumulator may be compared with any directly addressed byte or immediate data, and any indirect RAM location or working register can be compared with an immediate constant.

Example: The Accumulator contains 34H. Register 7 contains 56H. The first instruction in the sequence,

```
        CJNE    R7,#60H,NOT_EQ
;       ...     ....        ;       R7 = 60H.
NOT_EQ  JC      REQ_LOW     ;       IF R7 < 60H.
;       ...     ....        ;       R7 > 60H.
```

sets the carry flag and branches to the instruction at label NOT_EQ. By testing the carry flag, this instruction determines whether R7 is greater or less than 60H.

If the data being presented to Port 1 is also 34H, then the instruction,

```
WAIT:  CJNE  A,P1,WAIT
```

clears the carry flag and continues with the next instruction in sequence, since the Accumulator does equal the data read from P1. (If some other value was being input on P1, the program will loop at this point until the P1 data changes to 34H.)

CJNE A,direct,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	0 1 0 1	direct address	rel. address

Operation:

```
(PC) ← (PC) + 3
IF (A) < > (direct)
THEN
        (PC) ← (PC) + relative offset
IF (A) < (direct)
THEN.
        (C) ← 1
ELSE
        (C) ← 0
```

CJNE A,#data,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	0 1 0 0	immediate data	rel. address

Operation:

(PC) ← (PC) + 3
IF (A) < > *data*
THEN
(PC) ← (PC) + *relative offset*
IF (A) < *data*
THEN
(C) ← 1
ELSE
(C) ← 0

CJNE Rn,#data,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	1 r r r	immediate data	rel. address

Operation:

(PC) ← (PC) + 3
IF (R_n) < > *data*
THEN
(PC) ← (PC) + *relative offset*
IF (R_n) < *data*
THEN
(C) ← 1
ELSE
(C) ← 0

CJNE @Ri,#data,rel

Bytes: 3

Cycles: 2

Encoding:

1 0 1 1	0 1 1 i	immediate data	rel. address

Operation:

(PC) ← (PC) + 3
IF ((R_i)) < > *data*
THEN
(PC) ← (PC) + *relative offset*
IF ((R_i)) < *data*
THEN
(C) ← 1
ELSE
(C) ← 0

CLR A

Function: Clear Accumulator

Description: The Accumulator is cleared (all bits reset to zero). No flags are affected.

Example: The Accumulator contains 5CH (01011100B). The instruction,

CLR A

will leave the Accumulator set to 00H (00000000B).

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	0 1 0 0

Operation: CLR
(A) ← 0

CLR bit

Function: Clear bit

Description: The indicated bit is cleared (reset to zero). No other flags are affected. CLR can operate on the carry flag or any directly addressable bit.

Example: Port 1 has previously been written with 5DH (01011101B). The instruction,

CLR P1.2

will leave the port set to 59H (01011001B).

CLR C

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 0 1 1

Operation: CLR
(C) ← 0

CLR bit

Bytes: 2

Cycles: 1

Encoding:

1 1 0 0	0 0 1 0	bit address

Operation: CLR
(bit) ← 0

CPL A

Function: Complement Accumulator

Description: Each bit of the Accumulator is logically complemented (one's complement). Bits which previously contained a one are changed to a zero and vice-versa. No flags are affected.

Example: The Accumulator contains 5CH (01011100B). The instruction,

CPL A

will leave the Accumulator set to 0A3H (10100011B).

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	0 1 0 0

Operation: CPL
(A) ← ⌉ (A)

CPL bit

Function: Complement bit

Description: The bit variable specified is complemented. A bit which had been a one is changed to zero and vice-versa. No other flags are affected. CLR can operate on the carry or any directly addressable bit.

Note: When this instruction is used to modify an output pin, the value used as the original data will be read from the output data latch, *not* the input pin.

Example: Port 1 has previously been written with 5DH (01011101B). The instruction sequence,

CPL P1.1

CPL P1.2

will leave the port set to 5BH (01011011B).

CPL C

Bytes: 1

Cycles: 1

Encoding:

1 0 1 1	0 0 1 1

Operation: CPL
(C) ← ⌉ (C)

CPL bit

Bytes: 2

Cycles: 1

Encoding:

1 0 1 1	0 0 1 0	bit address

Operation: CPL
(bit) ← ⌉ (bit)

DA A

Function: Decimal-adjust Accumulator for Addition

Description: DA A adjusts the eight-bit value in the Accumulator resulting from the earlier addition of two variable (each in packed-BCD format), producing two four-bit digits. Any ADD or ADDC instruction may have been used to perform the addition.

If Accumulator bits 3-0 are greater than nine (xxx1010-xxx1111), or if the AC flag is one, six is added to the Accumulator, producing the proper BCD digit in the low-order nibble. This internal addition would set the carry flag if a carry-out of the low-order four-bit field propagated through all high-order bits, but it would not clear the carry flag otherwise.

If the carry flag is now set, or if the four high-order bits now exceed nine (1010xxx-111xxxx), these high-order bits are incremented by six, producing the proper BCD digit in the high-order nibble. Again, this would set the carry flag if there was a carry-out of the high-order bits, but wouldn't clear the carry. The carry flag thus indicates if the sum of the original two BCD variables is greater than 100, allowing multiple precision decimal addition. OV is not affected.

All of this occurs during the one instruction cycle. Essentially, this instruction performs the decimal conversion by adding 00H, 06H, 60H, or 66H to the Accumulator, depending on initial Accumulator and PSW conditions.

Note: DA A *cannot* simply convert a hexadecimal number in the Accumulator to BCD notation, nor does DA A apply to decimal subtraction.

Example: The Accumulator holds the value 56H (01010110B) representing the packed BCD digits of the decimal number 56. Register 3 contains the value 67H (01100111B) representing the packed BCD digits of the decimal number 67. The carry flag is set.. The instruction sequence,

```
ADDC    A,R3
DA      A
```

will first perform a standard two's-complement binary addition, resulting in the value 0BEH (10111110B) in the Accumulator. The carry and auxiliary carry flags will be cleared.

The Decimal Adjust instruction will then alter the Accumulator to the value 24H (00100100B), indicating the packed BCD digits of the decimal number 24, the low-order two digits of the decimal sum of 56, 67, and the carry-in. The carry flag will be set by the Decimal Adjust instruction, indicating that a decimal overflow occurred. The true sum 56, 67, and 1 is 124.

BCD variables can be incremented or decremented by adding 01H or 99H. If the Accumulator initially holds 30H (representing the digits of 30 decimal), the the instruction sequence,

```
ADD     A,#99H
DA      A
```

will leave the carry set and 29H in the Accumulator, since 30 + 99 = 129. The low-order byte of the sum can be interpreted to mean 30 – 1 = 29.

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 1 0 0

Operation:

```
DA
–contents of Accumulator are BCD
IF   [[(A3-0) > 9] ∨ [(AC) = 1]]
     THEN(A3-0) ← (A3-0) + 6
        AND
IF   [[(A7-4) > 9] ∨ [(C) = 1]]
     THEN(A7-4) ← (A7-4) + 6
```

DEC byte

Function: Decrement

Description: The variable indicated is decremented by 1. An original value of 00H will underflow to 0FFH. No flags are affected. Four operand addressing modes are allowed: accumulator, register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original data will be read from the output data latch, *not* the input pin.

Example: Register 0 contains 7FH (01111111B). Internal RAM locations 7EH and 7FH contain 00H and 40H, respectively. The instruction sequence,

```
DEC   @R0
DEC   R0
DEC   @R0
```

will leave register 0 set to 7EH and internal RAM locations 7EH and 7FH set to 0FFH and 3FH.

DEC A

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	0 1 0 0

Operation:
DEC
(A) ← (A) – 1

DEC Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	1 r r r

Operation:
DEC
(R_n) ← (R_n) – 1

DEC direct

Bytes: 2

Cycles: 1

Encoding:

0 0 0 1	0 1 0 1	direct address

Operation:
DEC
(direct) ← (direct) – 1

DEC @Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 0 1	0 1 1 i

Operation:
DEC
((R_i)) ← ((R_i)) – 1

DIV AB

Function: Divide

Description: DIV AB divides the unsigned eight-bit integer in the Accumulator by the unsigned eight-bit integer in register B.

The Accumulator receives the integer part of the quotient; register B receives the integer remainder. The carry and OV flags will be cleared.

Exception: if B had originally contained 00H, the values returned in the Accumulator and B-register will be undefined and the overflow flag will be set. The carry flag is cleared in any case.

Example: The Accumulator contains 251 (0FBH or 11111011B) and B contains 18 (12H or 00010010B). The instruction,

DIV AB

will leave 13 in the Accumulator (0DH or 00001101B) and the value 17 (11H or 00010001B) in B, since 251 = (13 x 18) + 17. Carry and OV will both be cleared.

Bytes: 1

Cycles: 4

Encoding:

1 0 0 0	0 1 0 0

Operation: DIV

$(A)_{15-8} \leftarrow (A)/(B)$

$(B)_{7-0}$

DJNZ <byte>,<rel-addr>

Function: Decrement and Jump if Not Zero

Description: DJNZ decrements the location indicated by 1, and branches to the address indicated by the second operand if the resulting value is not zero. An original value of 00H will underflow to 0FFH. No flags are affected. The branch destination would be computed by adding the signed relative-displacement value in the last instruction byte to the PC, after incrementing the PC to the first byte of the following instruction.

The location decremented may be a register or directly addressed byte.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: Internal RAM locations 40H, 50H, and 60H contain the values 01H, 70H, and 15H, respectively. The instruction sequence,

```
DJNZ    40H,LABEL_1
DJNZ    50H,LABEL_2
DJNZ    60H,LABEL_3
```

will cause a jump to the instruction at LABEL_2 with the values 00h, 6FH, and 15H in the three RAM locations. The first jump was *not* taken because the result was zero.

This instruction provides a simple was of executing a program loop a given number of times, or for adding a moderate time delay (from 2 to 512 machine cycles) with a single instruction. The instruction sequence,

```
        MOV     R2,#8
TOGGLE: CPL     P1.7
        DJNZ    R2,TOGGLE
```

will toggle P1.7 eight times, causing four output pulses to appear at bit 7 of output Port 1. Each pulse will last three machine cycles, two for DJNZ and one to alter the pin.

DJNZ Rn,rel

Bytes: 2

Cycles: 2

Encoding:

1 1 0 1	1 r r r	rel. address

Operation:

```
DJNZ
(PC) ← (PC) + 2
(Rn) ← (Rn) – 1
IF (Rn) > 0 or (Rn) < 0
   THEN
            (PC) ← (PC) + rel
```

DJNZ direct,rel

Bytes: 3

Cycles: 2

Encoding:

1 1 0 1	0 1 0 1	direct data	rel. address

Operation:

```
DJNZ
(PC) ← (PC) + 2
(direct) ← (direct) – 1
IF (direct) > 0 or (direct) < 0
   THEN
        (PC) ← (PC) + rel
```

INC <byte>

Function: Increment

Description: INC increments the indicated variable by 1. An original value of 0FFH will overflow to 00H. No flags are affected. Three addressing modes are allowed: register, direct, or register-indirect.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: Register 0 contains 7EH (01111110B). Internal RAM locations 7EH and 7FH contain 0FFH and 40H, respectively. The instruction sequence,

```
INC     @R0
INC     R0
INC     @R0
```

will leave register 0 set to 7FH and internal RAM locations 7EH and 7FH holding (respectively) 00H and 41H.

INC A

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 1 0 0

Operation: INC
(A) ← (A) + 1

INC Rn

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	1 r r r

Operation: INC
(R_n) ← (R_n) + 1

INC direct

Bytes: 2

Cycles: 1

Encoding:

0 0 0 0	0 1 0 1	direct address

Operation: INC
(direct) ← (direct) + 1

INC @Ri

Bytes: 1

Cycles: 1

Encoding:

0 0 0 0	0 1 1 i

Operation: INC
((R_i)) ← ((R_i)) + 1

INC DPTR

Function: Increment Data Pointer

Description: Increment the 16-bit data pointer by 1. A 16-bit increment (modulo 2^{16}) is performed; an overflow of the low-order byte of the data pointer (DPL) from 0FFH to 00H will increment the high-order byte (DPH). No flags are affected.

This is the only 16-bit register which can be incremented.

Example: Registers DPH and DPL contain 12H and 0FEH, respectively. The instruction sequence,

```
INC     DPTR
INC     DPTR
INC     DPTR
```

will change DPH and DPL to 13H and 01H.

Bytes: 1

Cycles: 2

Encoding:

1 0 1 0	0 0 1 1

Operation: INC

(DPTR) ← (DPTR) + 1

JB bit,rel

Function: Jump if Bit set

Description: If the indicated bit is a one, jump to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. *The bit tested is not modified.* No flags are affected.

Example: The data present at input port 1 is 11001010B. The Accumulator holds 56 (01010110B). The instruction sequence,

```
JB      P1.2,LABEL1
JB      ACC.2,LABEL2
```

will cause program execution to branch to the instruction at label LABEL2.

Bytes: 3

Cycles: 2

Encoding:

0 0 1 0	0 0 0 0	bit address	rel. address

Operation: JB

(PC) ← (PC) + 3

IF (bit) = 1

THEN

(PC) ← (PC) + rel

JBC bit,rel

Function: Jump if Bit is set and Clear bit

Description: If the indicated bit is a one, branch to the address indicated; otherwise proceed with the next instruction. *The bit will not be cleared if it is already a zero.* The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. No flags are affected.

Note: When this instruction is used to test an output pin, the value used as the original data will read from the output data latch, not the input pin.

Example: The Accumulator holds 56H (01010110B). The instruction sequence,

```
JBC     ACC.3,LABEL1
JBC     ACC.2,LABEL2
```

will cause program execution to continue at the instruction identified by the LABEL2, with the Accumulator modified to 52H (01010010B).

Bytes: 3

Cycles: 2

Encoding:

0 0 0 1	0 0 0 0	bit address	rel. address

Operation:

```
JBC
(PC) ← (PC) + 3
IF (bit) = 1
   THEN
(bit) ← 0
(PC) ← (PC) + rel
```

JC rel

Function: Jump if Carry is set

Description: If the carry flag is set, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. No flags are affected.

Example: The carry flag is cleared. The instruction sequence,

```
JC      LABEL1
CPL     C
JC      LABEL2
```

will set the carry and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0 1 0 0	0 0 0 0	rel. address

Operation:

```
JC
(PC) ← (PC) + 2
IF (C) = 1
   THEN
                (PC) ← (PC) + rel
```

JMP @A+DPTR

Function: Jump indirect

Description: Add the eight-bit unsigned contents of the Accumulator with the sixteen-bit data pointer, and load the resulting sum to the program counter. This will be the address for subsequent instruction fetches. Sixteen-bit addition is performed (modulo 2^{16}): a carry-out from the low-order eight bits propagates through the higher-order bits. Neither the Accumulator nor the Data Pointer is altered. No flags are affected.

Example: An even number from 0 to 6 is in the Accumulator. The following sequence of instructions will branch to one of four AJMP instructions in a jump table starting at JMP_TBL:

```
            MOV   DPTR,#JMP_TBL
            JMP   @A+DPTR
JMP_TBL:    AJMP  LABEL0
            AJMP  LABEL1
            AJMP  LABEL2
            AJMP  LABEL3
```

If the Accumulator equals 04H when starting this sequence, execution will jump to label LABEL2. Remember that AJMP is a two-byte instruction, so the jump instructions start at every other address.

Bytes: 1

Cycles: 2

Encoding:

0 1 1 1	0 0 1 1

Operation: JMP
(PC) ← (A) + (DPTR)

JNB bit,rel

Function: Jump if Bit Not set

Description: If the indicated bit is a zero, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the third instruction byte to the PC, after incrementing the PC to the first byte of the next instruction. *The bit tested is not modified.* No flags are affected.

Example: The data present at input port 1 is 11001010B. The Accumulator holds 56H (01010110B). The instruction sequence,

```
JNB     P1.3,LABEL1
JNB     ACC.3,LABEL2
```

will cause program execution to continue at the instruction at label LABEL2.

Bytes: 3

Cycles: 2

Encoding:

0 0 1 1	0 0 0 0	bit address	rel. address

Operation: JNB
(PC) ← (PC) + 3
IF (bit) = 0
THEN
(PC) ← (PC) + rel

JNC rel

Function: Jump if Carry Not set

Description: If the carry flag is a zero, branch to the address indicated; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice to point to the next instruction. The carry flag is not modified.

Example: The carry flag is set. The instruction sequence,

```
JNC     LABEL1
CPL     C
JNC     LABEL2
```

will clear the carry and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0 1 0 1	0 0 0 0	rel. address

Operation:

```
JNC
(PC) ← (PC) + 2
IF (C) = 0
   THEN
(PC) ← (PC) + rel
```

JNZ rel

Function: Jump if Accumulator Not Zero

Description: If any bit of the Accumulator is a one, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example: The Accumulator originally holds 00H. The instruction sequence,

```
JNZ     LABEL1
INC     A
JNZ     LABEL2
```

will set the Accumulator to 01H and continue at label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0 1 1 1	0 0 0 0	rel. address

Operation:

```
JNZ
(PC) ← (PC) + 2
IF A ≠ 0
   THEN  (PC) ← (PC) + rel
```

JZ rel

Function: Jump if Accumulator Zero

Description: If all bits of the Accumulator are zero, branch to the indicated address; otherwise proceed with the next instruction. The branch destination is computed by adding the signed relative-displacement in the second instruction byte to the PC, after incrementing the PC twice. The Accumulator is not modified. No flags are affected.

Example: The Accumulator originally holds 01H. The instruction sequence,

```
JZ      LABEL1
DEC     A
JZ      LABEL2
```

will change the Accumulator to 00H and cause program execution to continue at the instruction identified by the label LABEL2.

Bytes: 2

Cycles: 2

Encoding:

0 1 1 0	0 0 0 0	rel. address

Operation:

```
JZ
(PC) ← (PC) + 2
IF A = 0
   THEN (PC) ← (PC) + rel
```

LCALL addr16

Function: Long Call

Description: LCALL calls a subroutine located at the indicated address. The instruction adds three to the program counter to generate the address of the next instruction and then pushes the 16-bit result onto the stack (low byte first), incrementing the Stack Pointer by two. The high-order and low-order bytes of the PC are then loaded, respectively, with the second and third bytes of the LCALL instruction. Program execution continues with the instruction at this address. The subroutine may therefore begin anywhere in the full 64k-byte program memory address space. No flags are affected.

Example: Initially the Stack Pointer equals 07H. The label "SUBRTN" is assigned to program memory location 1234H. After executing the instruction,

```
LCALL   SUBRTN
```

at location 0123H, the Stack Pointer will contain 09H, internal RAM locations 08H and 09H will contain 26H and 01H, and the PC will contain 1235H.

Bytes: 3

Cycles: 2

Encoding:

0 0 0 1	0 0 1 0	addr15-addr8	addr7-addr0

Operation:

```
LCALL
(PC) ← (PC) + 3
(SP) ← (SP) + 1
((SP)) ← (PC7-0)
(SP) ← (SP) + 1
((SP)) ← (PC15-8)
(PC) ← addr15-0
```

LJMP addr16 (Implemented in 87C751 and 87C752 for in-circuit emulation only.)

Function: Long Jump

Description: LJMP causes an unconditional branch to the indicated address, by loading the high-order and low-order bytes of the PC (respectively) with the second and third instruction bytes. The destination may therefore be anywhere in the full 64k program memory address space. No flags are affected.

Example: The label "JMPADR" is assigned to the instruction at program memory location 1234H. The instruction,

LJMP JMPADR

at location 0123H will load the program counter with 1234H.

Bytes: 3

Cycles: 2

Encoding:

0 0 0 0	0 0 1 0	addr15-addr8	addr7-addr0

Operation: LJMP

(PC) ← $addr_{15-0}$

MOV <dest-byte>,<src-byte>

Function: Move byte variable

Description: The byte variable indicated by the second operand is copied into the location specified by the first operand. The source byte is not affected. No other register or flag is affected.

This is by far the most flexible operation. Fifteen combinations of source and destination addressing modes are allowed.

Example: Internal RAM location 30H holds 40H. The value of RAM location 40H is 10H. The data present at input port 1 is 11001010B (0CAH). The instruction sequence,

```
MOV   R0,#30H    ;R0 < = 30H
MOV   A,@R0      ;A < = 40H
MOV   R1,A       ;R1 < = 40H
MOV   B,@R1      ;B < = 10H
MOV   @R1,P1     ;RAM (40H) < = 0CAH
MOV   P2,P1      ;P2 #0CAH
```

leaves the value 30H in register 0, 40H in both the Accumulator and register 1, 10H in register B, and 0CAH (11001010B) both in RAM location 40H and output on port 2.

MOV A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	1 r r r

Operation: MOV

(A) ← (R_n)

***MOV A,direct**

Bytes: 2

Cycles: 1

Encoding:

1 1 1 0	0 1 0 1	direct address

Operation: MOV
(A) ← (direct)

MOV A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 1 1 0	0 1 1 i

Operation: MOV
(A) ← ((Ri))

MOV A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	0 1 0 0	immediate data

Operation: MOV
(A) ← #data

MOV Rn,A

Bytes: 1

Cycles: 1

Encoding:

1 1 1 1	1 r r r

Operation: MOV
(Rn) ← (A)

MOV Rn,direct

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	1 r r r	direct address

Operation: MOV
(Rn) ← (direct)

MOV Rn,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	1 r r r	immediate data

Operation: MOV
(Rn) ← #data

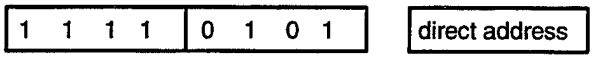
*MOV A,ACC is not a valid instruction.

MOV direct,A

Bytes: 2

Cycles: 1

Encoding:



Operation: MOV
(direct) ← (A)

MOV direct,Rn

Bytes: 2

Cycles: 2

Encoding:

Operation: MOV
(direct) ← (R_n)

MOV direct,direct

Bytes: 3

Cycles: 2

Encoding:

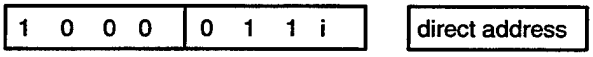
Operation: MOV
(direct) ← (direct)

MOV direct,@Ri

Bytes: 2

Cycles: 2

Encoding:



Operation: MOV
(direct) ← ((R_i))

MOV direct,#data

Bytes: 3

Cycles: 2

Encoding:

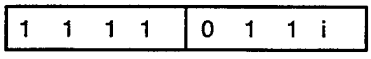
Operation: MOV
(direct) ← #data

MOV @Ri,A

Bytes: 1

Cycles: 1

Encoding:



Operation: MOV
((R_i)) ← (A)

MOV @Ri,direct

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	0 1 1 i	direct address

Operation: MOV
$((R_i)) \leftarrow$ (direct)

MOV @Ri,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 1	0 1 1 i	immediate data

Operation: MOV
$((R_i)) \leftarrow$ #data

MOV <dest-bit>,<src-bit>

Function: Move bit data

Description: The Boolean variable indicated by the second operand is copied into the location specified by the first operand. One of the operands must be the carry flag; the other may be any directly addressable bit. No other register or flag is affected.

Example: The carry flag is originally set. The data present at input Port 3 is 11000101B. The data previously written to output Port 1 is 35H (00110101B). The instruction sequence,

```
MOV   P1.3,C
MOV   C,P3.3
MOV   P1.2,C
```

will leave the carry cleared and change Port 1 to 39H (00111001B).

MOV C,bit

Bytes: 2

Cycles: 1

Encoding:

1 0 1 0	0 0 1 0	bit address

Operation: MOV
(C) $\leftarrow$ (bit)

MOV bit,C

Bytes: 2

Cycles: 2

Encoding:

1 0 0 1	0 0 1 0	bit address

Operation: MOV
(bit) $\leftarrow$ (C)

MOV DPTR,#data16

Function: Load Data Pointer with a 16-bit constant

Description: The Data Pointer is loaded with the 16-bit constant indicated. The 16-bit constant is loaded into the second and third bytes of the instruction. The second byte (DPH) is the high-order byte, while the third byte (DPL) holds the low-order byte. No flags are affected.

This is the only instruction which moves 16 bits of data at once.

Example: The instruction,

MOV DPTR,#1234H

will load the value 1234H into the Data Pointer: DPH will hold 12H and DPL will hold 34H.

Bytes: 3

Cycles: 2

Encoding:

1 0 0 1	0 0 0 0	immed. data15-8	immed. data7-0

Operation: MOV

(DPTR) ← (#data$_{15-0}$)

DPH ☐ DPL ← #data$_{15-8}$☐ #data$_{7-0}$

MOVC A,@A+<base-reg>

Function: Move Code byte

Description: The MOVC instructions load the Accumulator with a code byte, or constant from program memory. The address of the byte fetched is the sum of the original unsigned eight-bit Accumulator contents and the contents of a sixteen-bit base register, which may be either the Data Pointer or the PC. In the latter case, the PC is incremented to the address of the following instruction before being added with the Accumulator; otherwise the base register is not altered. Sixteen-bit addition is performed so a carry-out from the low-order eight bits may propagate through higher-order bits. No flags are affected.

Example: A value between 0 and 3 is in the Accumulator. The following instructions will translate the value in the Accumulator to one of four values defined by the DB (define byte) directive:

```
REL_PC:  INC   A
         MOVC  A,@A+PC
         RET
         DB    66H
         DB    77H
         DB    88H
         DB    99H
```

If the subroutine is called with the Accumulator equal to 01H, it will return with 77H in the Accumulator. The INC A before the MOVC instruction is needed to "get around" the RET instruction above the table. If several bytes of code separated the MOVC from the table, the corresponding number would be added to the Accumulator instead.

MOVC A,@A+DPTR

Bytes: 1

Cycles: 2

Encoding:

1 0 0 1	0 0 1 1

Operation: MOVC

(A) ← ((A) + (DPTR))

MOVC A,@A+PC

Bytes: 1

Cycles: 2

Encoding:

1 0 0 0	0 0 1 1

Operation: MOVC
(PC) ← (PC) + 1
(A) ← ((A) + (PC))

MOVX <dest-byte>,<src-byte> (Not implemented in the 8XC752 or 8XC752)

Function: Move External

Description: The MOVX instructions transfer data between the Accumulator and a byte of external data memory, hence the "X" appended to MOV. There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type, the contents of R0 or R1 in the current register bank provide an eight-bit address multiplexed with data on P0. Eight bits are sufficient for external I/O expansion decoding or for a relatively small RAM array. For somewhat larger arrays, port pins can be used to output higher-order address bits. These pins would be controlled by an output instruction preceding the MOVX.

In the second type of MOVX instruction, The Data Pointer generates a sixteen-bit address. P2 outputs the high-order eight address bits (the contents of DPH) while P0 multiplexes the low-order eight bits (DPL) with data. The P2 Special Function Register retains its previous contents while the P2 output buffers are emitting the contents of DPH. This form is faster and more efficient when accessing very large data arrays (up to 64k bytes), since no additional instructions are needed to set up the output ports.

It is possible in some situations to mix the two MOVX types. A large RAM array with its high-order address lines driven by P2 can be addressed via the Data Pointer, or with code to output high-order address bits to P2 followed by a MOVX instruction using R0 or R1.

Example: An external 256 byte RAM using multiplexed address/data lines is connected to the 8051 Port 0. Port 3 provides control lines for the external RAM. Ports 1 and 2 are used for normal I/O. Registers 0 and 1 contain 12H and 34H. Location 34H of the external RAM holds the value 56H. The instruction sequence,

```
MOVX  A,@R1
MOVX  @R0,A
```

copies the value 56H into both the Accumulator and external RAM location 12H.

MOVX A,@Ri

Bytes: 1

Cycles: 2

Encoding:

1 1 1 0	0 0 1 i

Operation: MOVX
(A) ← ((R_i))

MOVX A,@DPTR

Bytes: 1

Cycles: 2

Encoding:

1 1 1 0	0 0 0 0

Operation: MOVX
(A) ← ((DPTR))

MOVX @Ri,A

Bytes: 1

Cycles: 2

Encoding:

1 1 1 1	0 0 1 i

Operation: MOVX
$((R_i)) \leftarrow (A)$

MOVX @DPTR,A

Bytes: 1

Cycles: 2

Encoding:

1 1 1 1	0 0 0 0

Operation: MOVX
((DPTR)) ← (A)

MUL AB

Function: Multiply

Description: MUL AB multiplies the unsigned eight-bit integers in the Accumulator and register B. The low-order byte of the sixteen-bit product is left in the Accumulator, and the high-order byte in B. If the product is greater than 255 (0FFH) the overflow flag is set; otherwise it is cleared. The carry flag is always cleared.

Example: Originally the Accumulator holds the value 80 (50H). Register B holds the value 160 (0A0H).The instruction,

MUL AB

will give the product 12,800 (3200H), so B is changed to 32H (00110010B) and the Accumulator is cleared. The overflow flag is set, carry is cleared.

Bytes: 1

Cycles: 4

Encoding:

1 0 1 0	0 1 0 0

Operation: MUL
$(A)_{7-0} \leftarrow (A) \times (B)$
$(B)_{15-8}$

NOP

Function: No Operation

Description: Execution continues at the following instruction. Other than the PC, no registers or flags are affected.

Example: It is desired to produce a low-going output pulse on bit 7 of Port 2 lasting exactly 5 cycles. A simple SETB/CLR sequence would generate a one-cycle pulse, so four additional cycles must be inserted. This may be done (assuming are enabled) with the instruction sequence,

```
CLR     P2.7
NOP
NOP
NOP
NOP
SETB    P2.7
```

Bytes: 1

Cycles: 1

Encoding:

0	0	0	0	0	0	0	0

Operation: NOP
(PC) ← (PC) + 1

ORL <dest-byte>,<src-byte>

Function: Logical-OR for byte variables

Description: ORL performs the bitwise logical-OR operation between the indicated variables, storing the results in the destination byte. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

Note: When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.

Example: If the Accumulator holds 0C3H (11000011B) and R0 holds 55H (01010101B) then the instruction,

```
ORL   A,R0
```

will leave the Accumulator holding the value 0D7H (11010111B).

When the destination is a directly addressed byte, the instruction can set combinations of bits in any RAM location or hardware register. The pattern of bits to be set is determined by a mask byte, which may be either a constant data value in the instruction or a variable computed in the Accumulator at run-time. The instruction,

```
ORL   P1,#00110010B
```

will set bits 5, 4, and 1 of output Port 1.

ORL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0	1	0	0	1	r	r	r

Operation: ORL
(A) ← (A) ∨ (R_n)

ORL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 0 0	0 1 0 1	direct address

Operation: ORL
(A) ← (A) ∨ (direct)

ORL A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 1 0 0	0 1 1 i

Operation: ORL
(A) ← (A) ∨ ((Ri))

ORL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 0 0	0 1 0 0	immediate data

Operation: ORL
(A) ← (A) ∨ #data

ORL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 0 0	0 0 1 0	direct address

Operation: ORL
(direct) ← (direct) ∨ (A)

ORL direct,#data

Bytes: 3

Cycles: 2

Encoding:

0 1 0 0	0 0 1 1	direct address	immediate data

Operation: ORL
(direct) ← (direct) ∨ #data

ORL C,<src-bit>

Function: Logical-OR for bit variables

Description: Set the carry flag if the Boolean value is a logical 1; leave the carry in its current state otherwise. A slash ("/") preceding the operand in the assembly language indicates that the logical complement of the addressed bit is used as the source value, but the source bit itself is not affected. No other flags are affected.

Example: Set the carry flag if and only if P1.0 = 1, ACC.7 = 1, or OV = 0:

```
ORL   C,P1.0     ;LOAD CARRY WITH INPUT PIN P10
ORL   C,ACC.7    ;OR CARRY WITH THE ACC. BIT 7
ORL   C,/OV      ;OR CARRY WITH THE INVERSE OF OV.
```

ORL C,bit

Bytes: 2

Cycles: 2

Encoding:

0 1 1 1	0 0 1 0	bit address

Operation: ORL
(C) ← (C) ∨ (bit)

ORL C,/bit

Bytes: 2

Cycles: 2

Encoding:

1 0 1 0	0 0 0 0	bit address

Operation: ORL
(C) ← (C) ∨ ($\overline{\text{bit}}$)

POP direct

Function: Pop from stack

Description: The contents of the internal RAM location addressed by the Stack Pointer is read, and the Stack Pointer is decremented by one. The value read is then transferred to the directly addressed byte indicated. No flags are affected.

Example: The Stack Pointer originally contains the value 32H, and internal RAM locations 30H through 32H contain the values 20H, 23H, and 01H, respectively. The instruction sequence,

```
POP   DPH
POP   DPL
```

will leave the Stack Pointer equal to the value 30H and the Data Pointer set to 0123H. At this point the instruction,

```
POP   SP
```

will leave the Stack Pointer set to 20H. Note that in this special case the Stack Pointer was decremented to 2FH before being loaded with the value popped (20H).

Bytes: 2

Cycles: 2

Encoding:

1 1 0 1	0 0 0 0	direct address

Operation:

POP
(direct) ← ((SP))
(SP) ← (SP) – 1

PUSH direct

Function: Push onto stack

Description: The Stack Pointer is incremented by one. The contents of the indicated variable is then copied into the internal RAM location addressed by the Stack Pointer. Otherwise no flags are affected.

Example: On entering an interrupt routine the Stack Pointer contains 09H. The Data Pointer holds the value 0123H. The instruction sequence,

```
PUSH  DPL
PUSH  DPH
```

will leave the Stack Pointer set to 0BH and store 23H and 01H in internal RAM locations 0AH and 0BH, respectively.

Bytes: 2

Cycles: 2

Encoding:

1 1 0 0	0 0 0 0	direct address

Operation:

PUSH
(SP) ← (SP) + 1
((SP)) ← (direct)

RET

Function: Return from subroutine

Description: RET pops the high- and low-order bytes of the PC successively from the stack, decrementing the Stack Pointer by two. Program execution continues at the resulting address, generally the instruction immediately following an ACALL or LCALL. No flags are affected.

Example: The Stack Pointer originally contains the value 0BH. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,

RET

will leave the Stack Pointer equal to the value 09H. Program execution will continue at location 0123H.

Bytes: 1

Cycles: 2

Encoding:

0 0 1 0	0 0 1 0

Operation: RET

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

RETI

Function: Return from interrupt

Description: RETI pops the high- and low-order bytes of the PC successively from the stack, and restores the interrupt logic to accept additional interrupts at the same priority level as the one just processed. The Stack Pointer is left decremented by two. No other registers are affected; the PSW is not automatically restored to its pre-interrupt status. Program execution continues at the resulting address, which is generally the instruction immediately after the point at which the interrupt request was detected. If a lower- or same-level interrupt has been pending when the RETI instruction is executed, that one instruction will be executed before the pending interrupt is processed.

Example: The Stack Pointer originally contains the value 0BH. An interrupt was detected during the instruction ending at location 0122H. Internal RAM locations 0AH and 0BH contain the values 23H and 01H, respectively. The instruction,

RETI

will leave the Stack Pointer equal to 09H and return program execution to location 0123H.

Bytes: 1

Cycles: 2

Encoding:

0 0 1 1	0 0 1 0

Operation: RETI

$(PC_{15-8}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$
$(PC_{7-0}) \leftarrow ((SP))$
$(SP) \leftarrow (SP) - 1$

RL A

Function: Rotate Accumulator Left

Description: The eight bits in the Accumulator are rotated one bit to the left. Bit 7 is rotated into the bit 0 position. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

RL A

leaves the Accumulator holding the value 8BH (10001011B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding:

0	0	1	0	0	0	1	1

Operation: RL

$(A_{n+1}) \leftarrow (A_n)$, n = 0 – 6

(A0) ← (A7)

RLC A

Function: Rotate Accumulator Left through the Carry flag

Description: The eight bits in the Accumulator and the carry flag are together rotated one bit to the left. Bit 7 moves into the carry flag; the original state of the carry flag moves into the bit 0 position. No other flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction,

RLC A

leaves the Accumulator holding the value 8AH (10001010B) with the carry set.

Bytes: 1

Cycles: 1

Encoding:

0	0	1	1	0	0	1	1

Operation: RLC

$(A_{n+1}) \leftarrow (A_n)$, n = 0 – 6

(A0) ← (C)

(C) ← (A7)

RR A

Function: Rotate Accumulator Right

Description: The eight bits in the Accumulator are rotated one bit to the right. Bit 0 is rotated into the bit 7 position. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

RR A

leaves the Accumulator holding the value 0E2H (11100010B) with the carry unaffected.

Bytes: 1

Cycles: 1

Encoding:

0	0	0	0	0	0	1	1

Operation: RR

$(A_n) \leftarrow (A_{n+1})$, $n = 0 - 6$

(A7) ← (A0)

RRC A

Function: Rotate Accumulator Right through the Carry flag

Description: The eight bits in the Accumulator and the carry flag are together rotated one bit to the right. Bit 0 moves into the carry flag; the original state of the carry flag moves into the bit 7 position. No other flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B), and the carry is zero. The instruction,

RRC A

leaves the Accumulator holding the value 62 (01100010B) with the carry set.

Bytes: 1

Cycles: 1

Encoding:

0	0	0	1	0	0	1	1

Operation: RRC

$(A_n) \leftarrow (A_{n+1})$, $n = 0 - 6$

(A7) ← (C)

(C) ← (A0)

SETB <bit>

Function: Set Bit

Description: SETB sets the indicated bit to one. SETB can operate on the carry flag or any directly addressable bit. No other flags are affected.

Example: The carry flag is cleared. Output Port 1 has been written with the value 34H (00110100B). The instructions,

```
SETB   C
SETB   P1.0
```

will leave the carry flag set to 1 and change the data output on Port 1 to 35H (00110101B).

SETB C

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 0 1 1

Operation:
SETB
(C) ← 1

SETB bit

Bytes: 2

Cycles: 1

Encoding:

1 1 0 1	0 0 1 0	bit address

Operation:
SETB
(bit) ← 1

SJMP rel

Function: Short Jump

Description: Program control branches unconditionally to the address indicated. The branch destination is computed by adding the signed displacement in the second instruction byte to the PC, after incrementing the PC twice. Therefore, the range of destinations allowed is from 128 bytes preceding this instruction to 127 bytes following it.

Example: The label "RELADR" is assigned to an instruction at program memory location 0123H. The instruction,

```
SJMP   RELADR
```

will assemble into location 0100H. After the instruction is executed, the PC will contain the value 0123H.

(*Note:* Under the above conditions the instruction following SJMP will be at 102H. Therefore, the displacement byte of the instruction will be the relative offset (0123H-0102H) = 21H. Put another way, an SJMP with a displacement of 0FEH would be a one-instruction infinite loop.)

Bytes: 2

Cycles: 2

Encoding:

1 0 0 0	0 0 0 0	rel. address

Operation:
SJMP
(PC) ← (PC) + 2
(PC) ← (PC) + rel

SUBB A, <src-byte>

Function: Subtract with borrow

Description: SUBB subtracts the indicated variable and the carry flag together from the Accumulator, leaving the result in the Accumulator. SUBB sets the carry (borrow) flag if a borrow is needed for bit 7, and clears C otherwise. (If C was set *before* executing a SUBB instruction, this indicates that a borrow was needed for the previous step in a multiple precision subtraction, so the carry is subtracted from the Accumulator along with the source operand.) AC is set if a borrow is needed for bit 3, and cleared otherwise. OV is set if a borrow is needed into bit 6, but not into bit 7, or into bit 7, but not bit 6.

When subtracting signed integers OV indicates a negative number produced when a negative value is subtracted from a positive value, or a positive result when a positive number is subtracted from a negative number.

The source operand allows four addressing modes: register, direct, register-indirect, or immediate.

Example: The Accumulator holds 0C9H (11001001B), register 2 holds 54H (01010100B), and the carry flag is set. The instruction,

SUBB A,R2

will leave the value 74H (01110100B) in the Accumulator, with the carry flag and AC cleared but OV set.

Notice that 0C9H minus 54H is 75H The difference between this and the above result is due to the carry (borrow) flag being set before the operation. If the state of the carry is not known before starting a single or multiple-precision subtraction, it should be explicitly cleared by a CLR C instruction

SUBB A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 0 0 1	1 r r r

Operation: SUBB
(A) ← (A) – (C) – (R_n)

SUBB A,direct

Bytes: 2

Cycles: 1

Encoding:

1 0 0 1	0 1 0 1	direct address

Operation: SUBB
(A) ← (A) – (C) – (direct)

SUBB A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 0 0 1	0 1 1 i

Operation: SUBB
(A) ← (A) – (C) – (R_i)

SUBB A,#data

Bytes: 2

Cycles: 1

Encoding:

1 0 0 1	0 1 0 0	immediate data

Operation: SUBB
(A) ← (A) – (C) – (#data)

SWAP A

Function: Swap nibbles within the Accumulator

Description: SWAP A interchanges the low- and high-order nibbles (four-bit fields) of the Accumulator (bits 3-0 and bits 7-4). The operation can also be thought of as a four-bit rotate instruction. No flags are affected.

Example: The Accumulator holds the value 0C5H (11000101B). The instruction,

SWAP A

leaves the Accumulator holding the value 5CH (01011100B).

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 1 0 0

Operation: SWAP
$(A_{3-0}) \rightleftarrows (A_{7-4})$

XCH A,<byte>

Function: Exchange Accumulator with byte variable

Description: XCH loads the Accumulator with the contents of the indicated variable, at the same time writing the original Accumulator contents to the indicated variable. The source/destination operand can use register, direct, or register-indirect addressing.

Example: R0 contains the address 20H. The Accumulator holds the value 3FH (00111111B). Internal RAM location 20H holds the value 75H (01110101B). The instruction,

XCH A,@R0

will leave the RAM location 20H holding the values 3FH (00111111B) and 75H (01110101B) in the Accumulator.

XCH A,Rn

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	1 r r r

Operation: XCH
$(A) \rightleftarrows (R_n)$

XCH A,direct

Bytes: 2

Cycles: 1

Encoding:

1 1 0 0	0 1 0 1	direct address

Operation: XCH
(A) ⇄ (direct)

XCH A,@Ri

Bytes: 1

Cycles: 1

Encoding:

1 1 0 0	0 1 1 i

Operation: XCH
$(A) \rightleftarrows ((R_i))$

XCHD A,@Ri

Function: Exchange Digit

Description: XCHD exchanges the low-order nibble of the Accumulator (bits 3-0), generally representing a hexadecimal or BCD digit, with that of the internal RAM location indirectly addressed by the specified register. The high-order nibbles (bits 7-4) of each register are not affected. No flags are affected.

Example: R0 contains the address 20H. The Accumulator holds the value 36H (00110110B). Internal RAM location 20H holds the value 75H (01110101B). The instruction,

XCHD A,@R0

will leave RAM location 20H holding the value 76H (01110110B) and 35H (00110101B) in the Accumulator.

Bytes: 1

Cycles: 1

Encoding:

1 1 0 1	0 1 1 i

Operation: XCHD

$(A_{3-0}) \rightleftarrows ((Ri_{3-0}))$

XRL <dest-byte>,<src-byte>

Function: Logical Exclusive-OR for byte variables

Description: XRL performs the bitwise logical Exclusive-OR operation between the indicated variables, storing the results in the destination. No flags are affected.

The two operands allow six addressing mode combinations. When the destination is the Accumulator, the source can use register, direct, register-indirect, or immediate addressing; when the destination is a direct address, the source can be the Accumulator or immediate data.

(*Note:* When this instruction is used to modify an output port, the value used as the original port data will be read from the output data latch, *not* the input pins.)

Example: If the Accumulator holds 0C3H (11000011B) and register 0 holds 0AAH (10101010B) then the instruction,

XRL A,R0

will leave the Accumulator holding the value 69H (01101001B).

When the destination is a directly addressed byte, this instruction can complement combinations of bits in any RAM location or hardware register. The pattern of bits to be complemented is then determined by a mask byte, either a constant contained in the instruction or a variable computed in the Accumulator at run-time. The instruction,

XRL P1,#00110001B

will complement bits 5, 4, and 0 of output Port 1.

XRL A,Rn

Bytes: 1

Cycles: 1

Encoding:

0 1 1 0	1 r r r

Operation: XRL
(A) ← (A) ⩛ (R_n)

XRL A,direct

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 1 0 1	direct address

Operation: XRL
(A) ← (A) ⩛ (direct)

XRL A,@Ri

Bytes: 1

Cycles: 1

Encoding:

0 1 1 0	0 1 1 i

Operation: XRL
(A) ← (A) ⩛ (R_i)

XRL A,#data

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 1 0 0	immediate data

Operation: XRL
(A) ← (A) ⩛ #data

XRL direct,A

Bytes: 2

Cycles: 1

Encoding:

0 1 1 0	0 0 1 0	direct address

Operation: XRL
(direct) ← (direct) ⩛ (A)

XRL direct,#data

Bytes: 3

Cycles: 2

Encoding:

0 1 1 0	0 0 1 1	direct address	immediate data

Operation: XRL
(direct) ← (direct) ⩛ #data

APPENDIX C. DATASHEETS

The following Pages include manufacturer data sheets from the following companies:

- *UTMC*
  - *UT69RH051*
  - *UT28F64*
  - *UT67164*
- *MAXIM*
  - *MAX 232*
  - *MAX 233*
- *Harris*
  - *HS-82C55ARH*

Military Standard Products

UT69RH051 MicroController

Product Brief

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

March 199

FEATURES

- ☐ Three 16-bit timer/counters
  - High speed output
  - Compare/capture
  - Pulse width modulator
  - Watchdog timer capabilities
- ☐ 256 bytes of on-chip data RAM
- ☐ 32 programmable I/O lines
- ☐ 7 interrupt sources
- ☐ Programmable serial channel with:
  - Framing error detection
  - Automatic address recognition
- ☐ TTL and CMOS compatible logic levels
- ☐ 64K external data and program memory space
- ☐ MCS®-51 fully compatible instruction set
- ☐ Flexible clock operation
  - 1Hz to 20MHz with external clock
  - 2MHz to 20MHz using internal oscillator with external crystal
- ☐ Radiation-hardened process and design; total dose irradiation testing MIL-STD-883 Method 1019
  - Total dose: 1.0E6 rads(Si)
  - Single event upset: <25.6E-6 errors/device-day
  - Latchup immune
- ☐ Post-radiation AC/DC performance characteristics guaranteed to MIL-STD-883 Method 1019 testing at 1.0E6 rads (Si)
- ☐ Built on low-power, 1.2µ CMOS process
- ☐ Packaging options:
  - 40-pin DIP
  - 44-lead flatpack

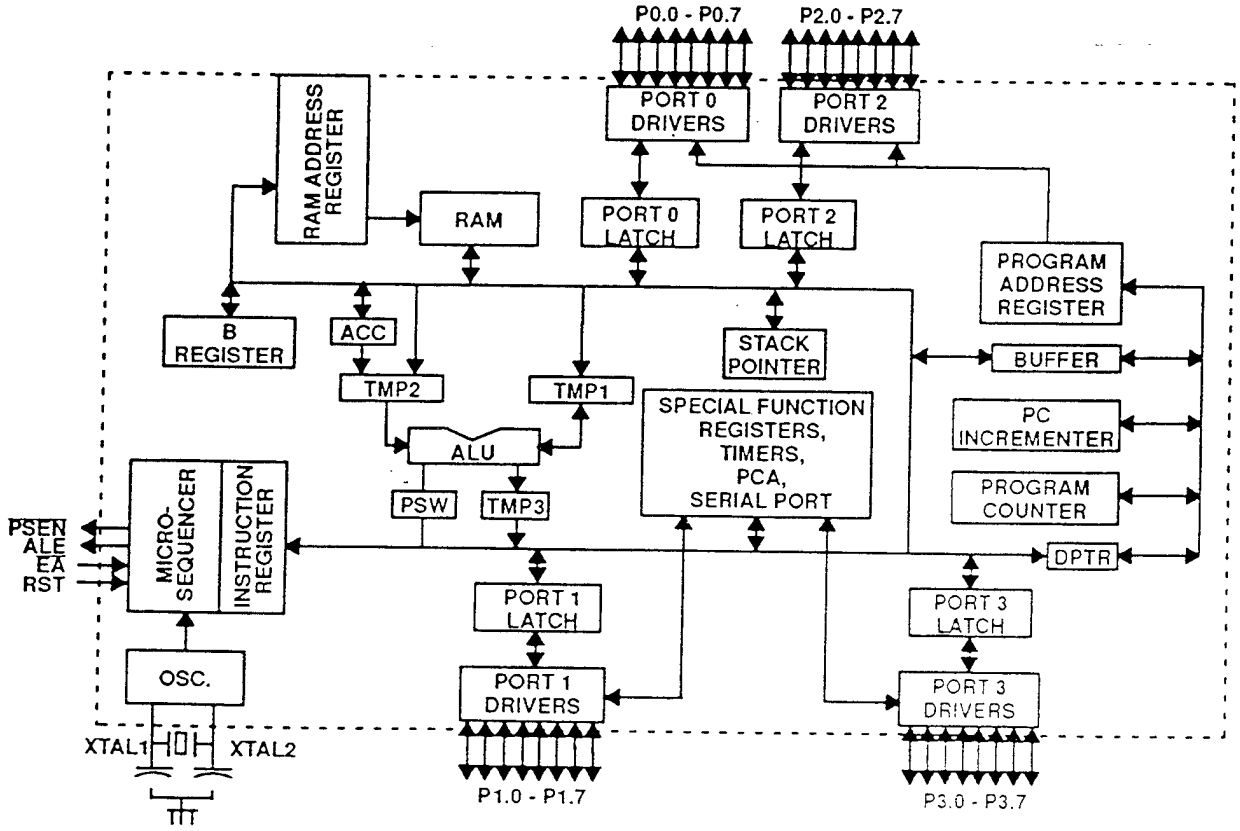


Figure 1. UT69RH051 MicroController Block Diagram

1.0 INTRODUCTION

The UT69RH051 is a radiation-tolerant 8-bit microcontroller that is pin equivalent to the Intel 8XC51FC microcontroller. The UT69RH051's static design allows operation from 1Hz to 20MHz. This product brief will describe hardware and software interfaces to the UT69RH051.

2.0 SIGNAL DESCRIPTION

V_{DD}: +5V Supply voltage

V_{SS}: Circuit Ground

Port 0 (P0.0 - P0.7): Port 0 is an 8-bit port. Its pins are used as the low-order multiplexed address and data bus during accesses to external program and data memory. Port 0 pins use strong internal pullups when emitting 1's, and are TTL compatible.

Port 1 (P1.0 - P1.7): Port 1 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 1 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 1 pins have the alternate uses shown in table 1.

Port 2 (P2.0 - P2.7): Port 2 is an 8-bit port. Its pins are used as the high-order address bus during accesses to external Program Memory and during accesses to external Data Memory that uses 16-bit addresses (i.e., MOVX@DPTR). It uses strong internal pullups when emitting 1's in this mode. During operations that do not require a 16-bit address, Port 2 emits the contents of the P2 Special Function Registers (SFR). The pins have internal pullups and can drive TTL loads.

Port 3 (p3.0 - p3.7): Port3 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 3 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 3 pins have the alternate uses shown in table 2.

Table 1. Port 1 Alternate Functions

Port Pin	Alternate Name	Alternate Function
P1.0	T2	External clock input to Timer/ Counter 2
P1.1	T2EX	Timer/Counter 2 Capture/Reload trigger and direction control
P1.2	ECI	External count input to PCA
P1.3	CEX0	External I/O for PCA capture/ compare Module 0
P1.4	CEX1	External I/O for PCA capture/ compare Module 1
P1.5	CEX2	External I/O for PCA capture/ compare Module 2
P1.6	CEX3	External I/O for PCA capture/ compare Module 3
P1.7	CEX4	External I/O for PCA capture/ compare Module 4

Table 2. Port 3 Alternate Functions

Port Pin	Alternate Name	Alternate Function
P3.0	RXD	Serial port input
P3.1	TXD	Serial port output
P3.2	$\overline{INT0}$	External interrupt 0
P3.3	$\overline{INT1}$	External interrupt 1
P3.4	T0	External clock input for Timer 0
P3.5	T1	External clock input for Timer 1
P3.6	$\overline{WR}$	External Data Memory write strobe
P3.7	$\overline{RD}$	External Data Memory read strobe

RST: Reset Input. A high on this input for one oscillator period while the oscillator is running resets the device. All ports and SFRs reset to their default conditions. Internal data memory is undefined after reset. Program execution begins within 12 oscillator periods (one machine cycle) after the RST signal is brought low. RST contains an internal pulldown resistor to allow implementing power-up reset with only an external capacitor.

ALE: Address Latch Enable. The ALE output is a pulse for latching the low byte of the address during accesses to external memory. In normal operation the ALE pulse is output every sixth oscillator cycle and may be used for external timing or clocking. However, during each access to external Data Memory (MOVX instruction), one ALE pulse is skipped.

$\overline{\text{PSEN}}$: Program Store Enable. This active low signal is the read strobe to the external program memory. $\overline{\text{PSEN}}$ is activated every sixth oscillator cycle except that two $\overline{\text{PSEN}}$ activations are skipped during external data memory accesses.

$\overline{\text{EA}}$: External Access Enable. This pin should be strapped to V_{SS} (Ground) for the UT69RH051.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

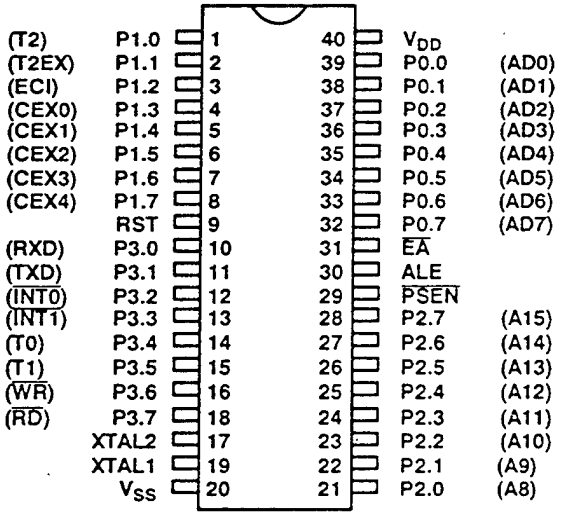


Figure 2. UT69RH051 Pin Connections

2.1 Hardware/Software Interface

2.1.1 Memory

The UT69RH051 has a separate address space for Program and Data Memory. Internally the UT69RH051 contains 25(bytes of Data Memory. It can address up to 64Kbytes of external Data Memory and 64Kbytes of external Program Memory.

2.1.1.1 Program Memory

There is no internal program memory in the UT69RH051. All program memory is accessed as external through ports P0 and P2. The $\overline{\text{EA}}$ pin must be tied to V_{SS} (ground) to enable access to external locations 0000_H through $7FFF_H$.

2.1.1.2 Data Memory

The UT69RH051 implements 256 bytes of internal data RAM. The upper 128 bytes of this RAM occupy a parallel address space to the SFRs. The CPU determines if the internal access to an address above 7FH is to the upper 128 bytes of RAM or to the SFR space by the addressing mode of the instruction. If direct addressing is used, the access is to the SFR space. If indirect addressing is used, the access i to the internal RAM. Stack operations are indirectly addressed so the upper portion of RAM can be used as stacl space. Figure 3 shows the organization of the internal Data Memory.

The first 32 bytes are reserved for four register banks of eight bytes each. The processor uses one of the four banks as its working registers depending on the RS1 and RS0 bits in the PSW SFR. At reset, bank 0 is selected. If four registe banks are not required, use the unused banks as general purpose scratch pad memory. The next 16 bytes (128 bits) are individually bit addressable. The remaining bytes are byte addressable and can be used as general purpose scratcl pad memory. For addresses 0 - $7F_H$, use either direct or indirect addressing. For addresses larger than $7F_H$, use only indirect addressing.

In addition to the internal Data Memory, the processor can access 64 Kbytes of external Data Memory. The MOVX instruction accesses external Data Memory.

2.1.2 Special Function Registers

Table 3 contains the SFR memory map. Unoccupied addresses are not implemented on the device. Read accesses to these addresses will return unknown values and write accesses will have no effect.

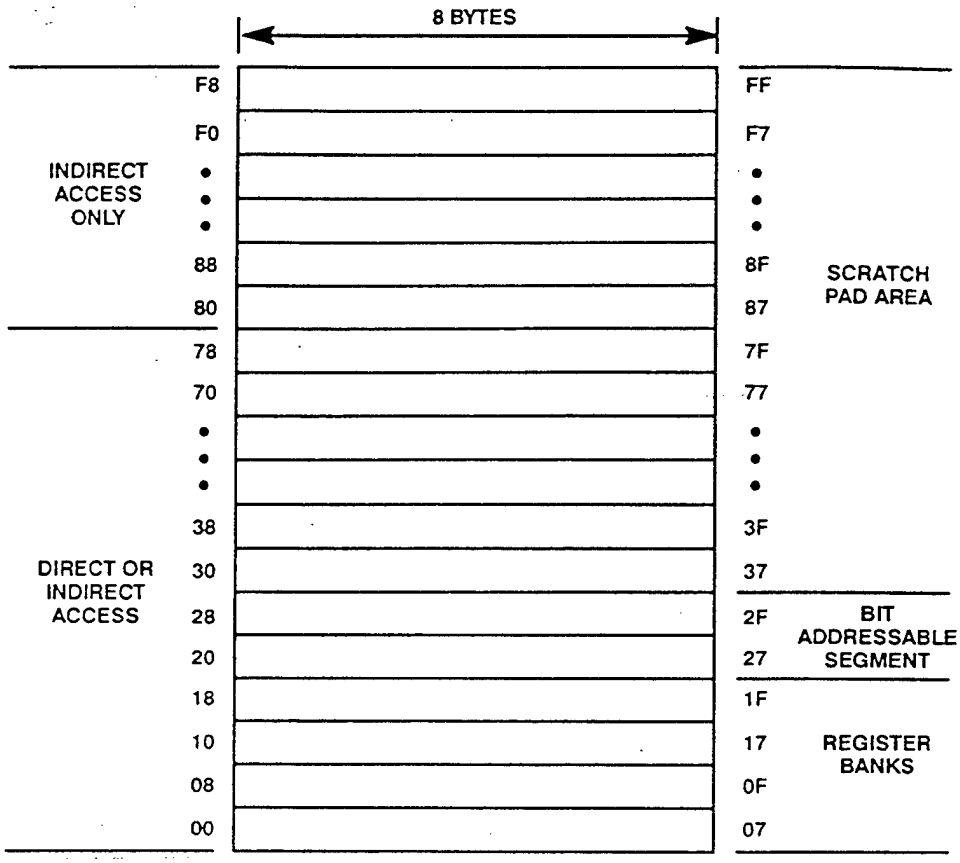


Figure 3. Internal Data Memory Organization

2.1.3 Reset

The reset input is the RST pin. To reset, hold a the RST pin high for a minimum of 24 oscillator period while the oscillator is running. The CPU generates an internal reset from the external signal. The ports pins are driven to the reset state as soon as a valid high is detected on the RST pin.

While RST is high, $\overline{PSEN}$, ALE, and the port pins are pulled weakly high. All SFRs are reset to their reset values as shown in table 3. The internal Data Memory content is indeterminate.

The processor will begin operation one machine cycle after the RST line is brought low. A memory access occurs immediately after the RST line is brought low, but the data is not brought into the processor. The memory access repeats on the next machine cycle and actual processing begins at that time.

2.1.4 Instruction Set

The instruction set for the UT69RH051 is compatible to the Intel MCS-51 instruction set used on the 8XC51FC.

Table 3. SFR Memory Registers

F8		CH 00000000	CCAP0H XXXXXXXX	CCAP1H XXXXXXXX	CCAP2H XXXXXXXX	CCAP3H XXXXXXXX	CCAP4H XXXXXXXX		FF
F0	B 00000000								F7
E8		CL 00000000	CCAP0L XXXXXXXX	CCAP1L XXXXXXXX	CCAP2L XXXXXXXX	CCAP3L XXXXXXXX	CCAP4L XXXXXXXX		EF
E0	ACC 00000000								E7
D8	CCON 00X00000	CMOD OOXXX000	CCAPM0 X00000000	CCAPM1 X00000000	CCAPM2 X00000000	CCAPM3 X00000000	CCAPM4 X00000000		DF
D0	PSW 00000000								D7
C8	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0									C7
B8	IP X0000000	SADEN 00000000							BF
B0	P3 11111111							IPH X00000000	B7
A8	IE 00000000	SADDR 00000000							AF
A0	P2 11111111								A7
98	SCON 00000000	SBUF XXXXXXXX							9F
90	P1 11111111								97
88	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00XX00XX	87

Notes:
1. Values shown are the reset values of the registers.
2. X = undefined.

3.0 RADIATION HARDNESS

The UT69RH051 incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
Dose Rate Upset	≤ 4µs pulsewidth	1.0E8	rads(Si)/sec
Dose Rate Survival	20ns pulsewidth	1.0E10	rads(Si)/sec
LET Threshold	-55°C to +125°C	36	MeV-cm^2/mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm^2

Note:
1. The UT69RH051 will not latchup during radiation exposure under recommended operating conditions.

4.0 ABSOLUTE MAXIMUM RATINGS [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	DC Supply Voltage	-0.5 to 7.0	V
$V_{I/O}$	Voltage on Any Pin	-0.5 to V_{DD}+3V	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Power Dissipation	750	mW
T_J	Maximum Junction Temperature	175	°C
Θ_{JC}	Thermal Resistance, Junction-to-Case [2]	10	°C/W
I_I	DC Input Current	±10	mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

6.0 DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

V_{DD} = 5.0V ±10%; TA = -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level Input Voltage		-0.5	.8	V
V_{IH}	High-level Input Voltage (except XTAL2, RST, $\overline{EA}$)		2.0	V_{DD}+0.3	V
V_{IH1}	High-level Input Voltage (XTAL, RST)		3.85	V_{DD}+0.3	V
V_{OL}	Low-level Output Voltage[1] (Ports 1, 2 and 3)	I_{OL} = 100µA		0.3	V
		I_{OL} = 1.6mA		0.45	V
		I_{OL} = 3.5mA		1.0	V
V_{OL1}	Low-level Output Voltage[1] (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)	I_{OL} = 200µA		0.3	V
		I_{OL} = 3.2mA		0.45	V
		I_{OL} = 7.0mA		1.0	V
V_{OH}	High-level Output Voltage (Ports 1, 2, and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	I_{OH} = -10µA	4.2		V
		I_{OH} = -30µA	3.8		V
		I_{OH} = -60µA	3.0		V
V_{OH1}	High-level Output Voltage (Port 0 in External Bus Mode)	I_{OH} = -200µA	4.2		V
		I_{OH} = -3.2mA	3.8		V
		I_{OH} = -7.0mA	3.0		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)	V_{IN} = 0.45V		-50	µA
I_{LI}	Input Leakage Current (Port 0)	V_{IN} = V_{IL} or V_{IH}		± 10	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)	V_{IN} = 2V		-650	µA
C_{IO}	Pin Capacitance	@ 1MHZ, 25°C		10	pF
I_{CC}	Power Supply Current: (Running at 16MHz)	Note 2		52	mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883.

1. Under steady state (non-transient) conditions, I_{OL} must be limited externally as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port-
   Port 0: 26mA
   Ports 1, 2, & 3: 15mA
   Maximum total I_{OL} for all output pins: 71mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. See figures 4, 5, and 6 for test conditions.

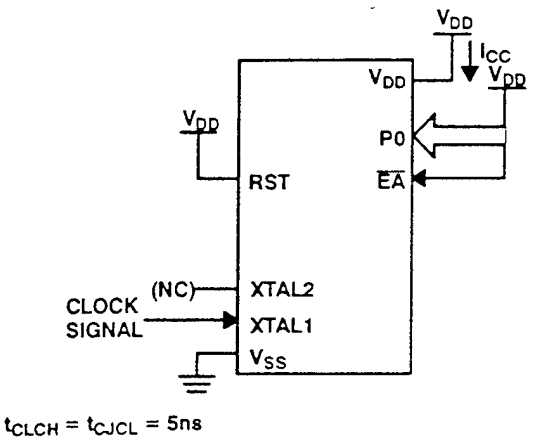


Figure 4. I_{DD} Test Condition, Active Mode
All other pins disconnected

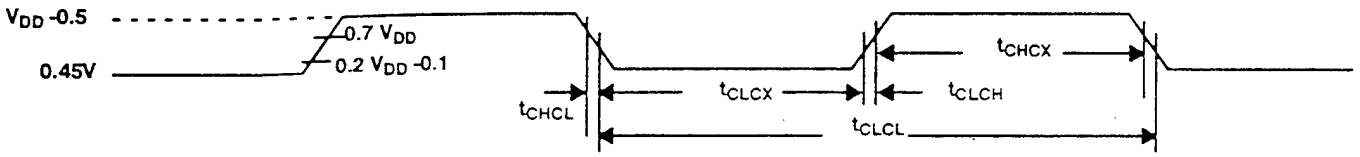


Figure 5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

7.0 AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{CLCL}	Clock Period	50		ns
$1/t_{CLCL}$	Oscillator Frequency		16	MHz
t_{LHLL}	ALE Pulse Width	$2\,t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL}-40		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL}-30		ns
t_{LLIV}	ALE Low to Valid Instruction In		$4\,t_{CLCL}$-100	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	t_{CLCL}-30		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	$3\,t_{CLCL}$-45		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		$3\,t_{CLCL}$-105	ns
t_{PXIX}	Input Instruction Hold after $\overline{PSEN}$	0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		t_{CLCL}-25	ns
t_{AVIV}	Address to Valid Instruction In		$5\,t_{CLCL}$-105	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	$6\,t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	$6\,t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		$5\,t_{CLCL}$-165	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		$2\,t_{CLCL}$-60	ns
t_{LLDV}	ALE Low Valid Data In		$8\,t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		$9\,t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	$3\,t_{CLCL}$-50	$3\,t_{CLCL}$+50	ns
t_{AVWL}	Address Valid to $\overline{WR}$ Low	$4\,t_{CLCL}$-130		ns
t_{QVWX}	Data Valid Before $\overline{WR}$	t_{CLCL}-50		ns
t_{WHQX}	Data Hold After $\overline{WR}$	t_{CLCL}-50		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	$7\,t_{CLCL}$-150		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	t_{CLCL}-40	t_{CLCL}+40	ns

Note:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

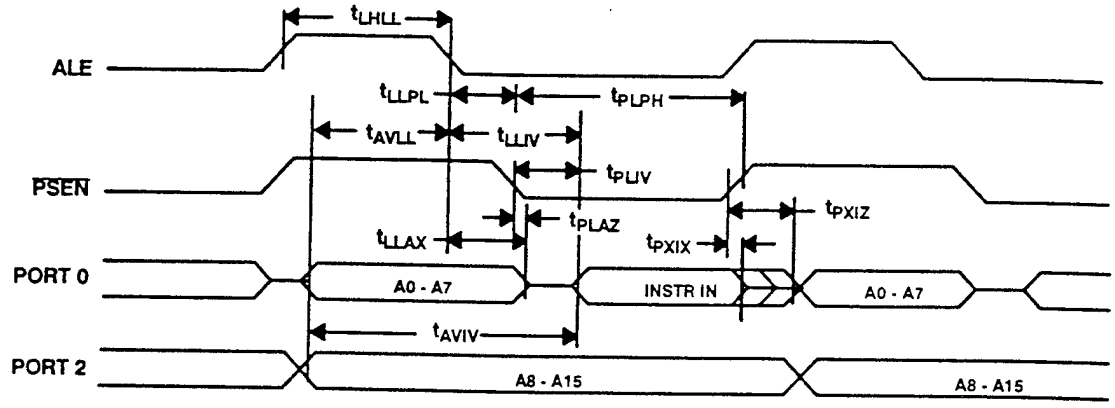


Figure 6. External Program Memory Read Timing Waveforms

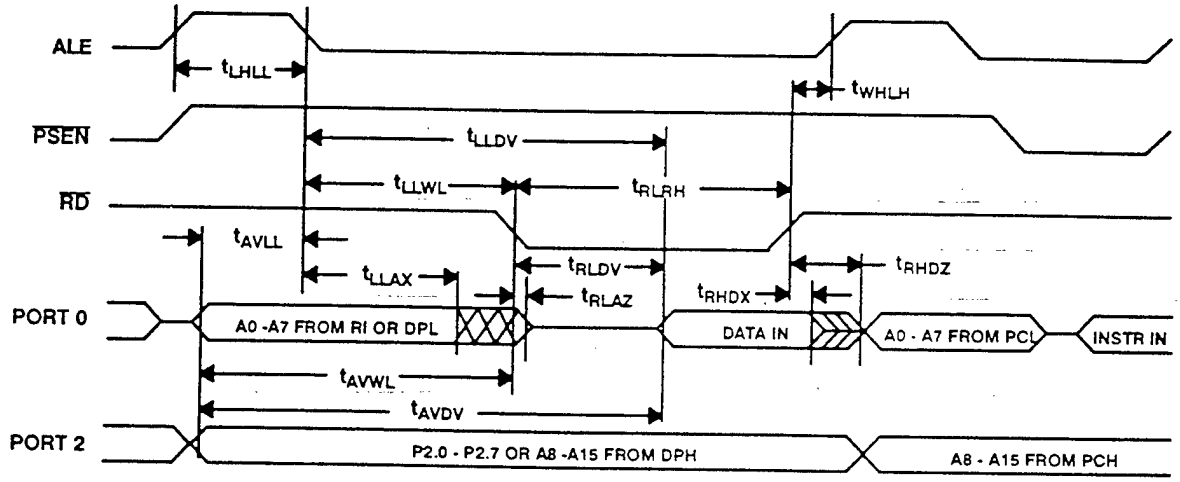


Figure 7. External Data Memory Read Cycle Waveforms

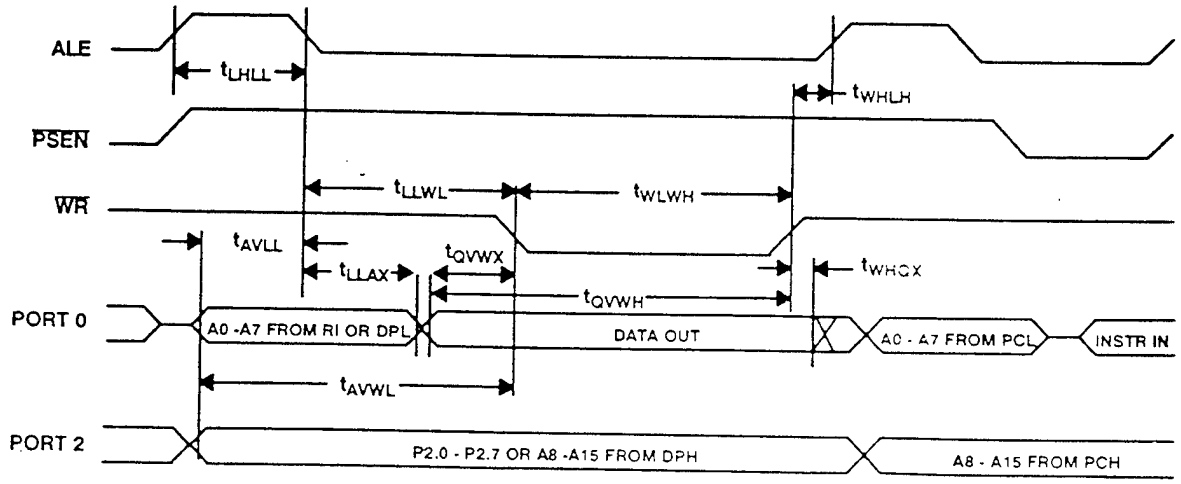


Figure 8. External Data Memory Write Cycle Waveforms

8.0 SERIAL PORT TIMING CHARACTERISTICS

(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{XLXL}	Serial Port Clock Period	12 t_{CLCL}-10	12 t_{CLCL}+10	ns
t_{QVXH}	Output Data Setup to Clock Rising Edge	10 t_{CLCL}-133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	2 t_{CLCL}-70		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		10 t_{CLCL}-133	ns

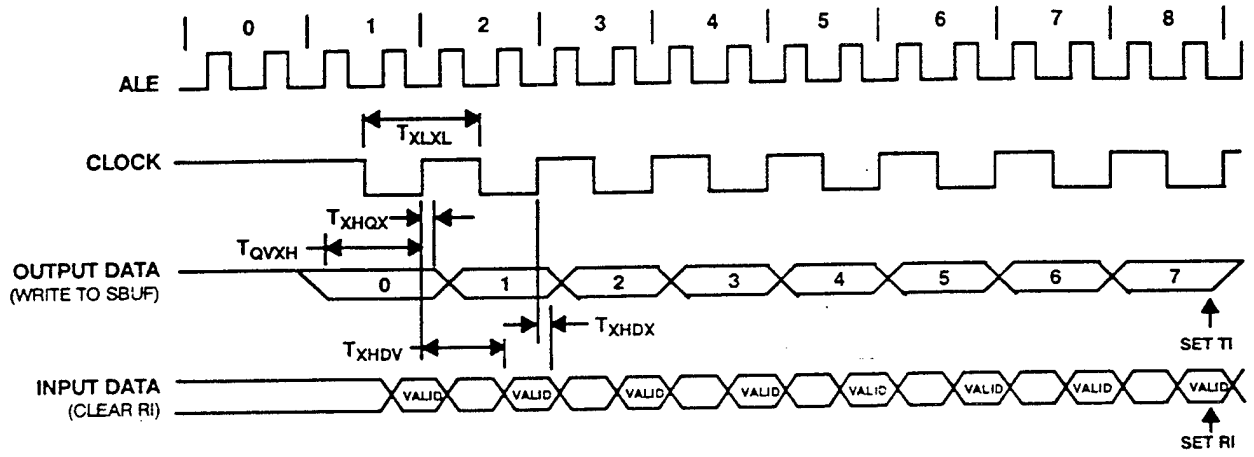


Figure 9. Serial Port Timing Waveforms

9.0 EXTERNAL CLOCK DRIVE TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
1/t_{CLCL}	Oscillator Frequency		16	MHz
t_{CHCX}	High Time	20		ns
t_{CLCX}	Low Time	20		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

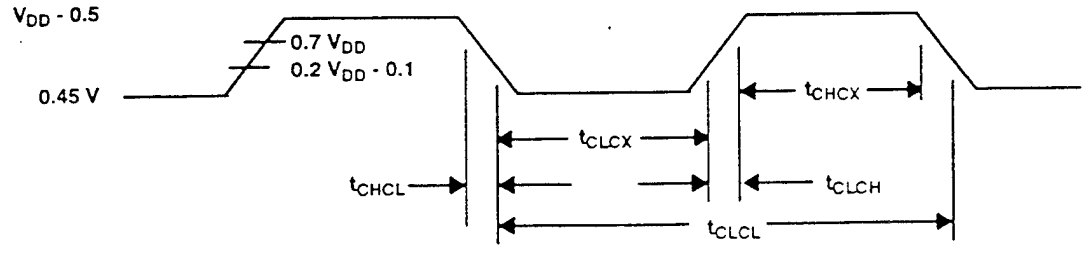
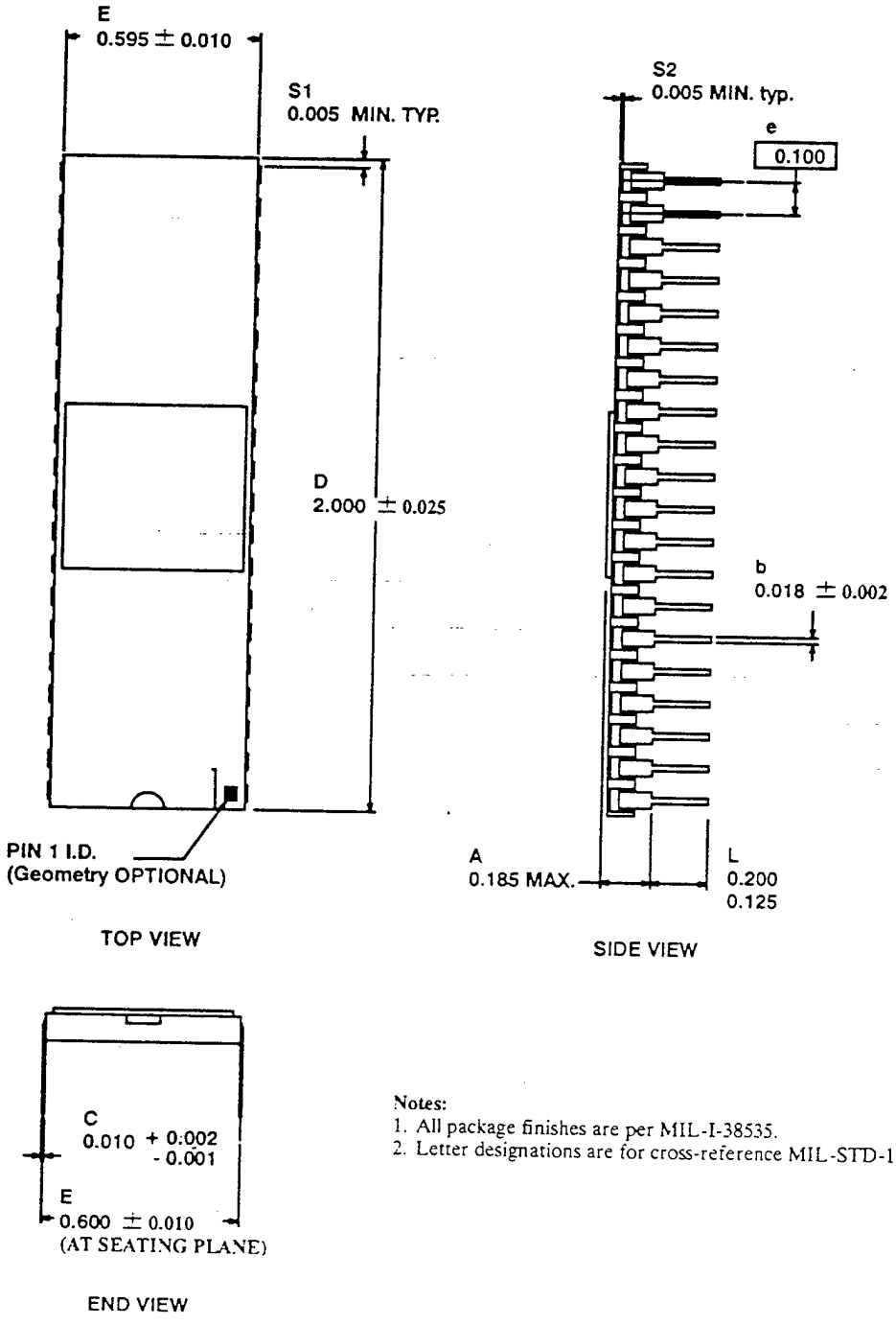


Figure 10. External Clock Drive Timing Waveforms

10.0 PACKAGING



Notes:
1. All package finishes are per MIL-I-38535.
2. Letter designations are for cross-reference MIL-STD-1835.

Figure 11. 40-pin Side-Brazed DIP

TBD

Figure 12. 44-Lead Flatpack

APPENDIX A
Difference Between Intel 8XC51FC and UTMC69RH051

There are a few areas in which the UT69RH051 differs from the 8XC51FC. These differences will be covered in this section. In this discussion, 8XC51FC will be used generically to refer to all speed grades of the Intel 8XC51FC family, including the 20MHz 8XC51FC-1.

1.0 RESET

The UT69RH051 requires the RST input to be held high for at least 24 oscillator periods to guarantee the reset is completed in the chip. Also, the port pins are reset asynchronously as soon as the RST pin is pulled high. On the UT69RH051 all portions of the chip are reset synchronously when the RST pin is high during a rising edge of the input clock. When coming out of reset, the 8XC51FC takes 1 to 2 machine cycles to begin driving ALE and $\overline{PSEN}$ immediately after the RST is removed but the access during the first machine cycle after reset is ignored by the processor. The second cycle will repeat the access and processing will begin.

2.0 POWER SAVING MODES OF OPERATION

2.1 Idle Mode

Idle mode and the corresponding control bit in the PCON SFR have not been implemented in the UT69RH051. Setting the idle control bit will have no effect.

2.2 Power Down Mode

Power down mode and the corresponding control bit in the PCON register have not been implemented in the UT69RH051. Setting the power down control bit will have no effect. Also, the Power Off Flag in the PCON has not been implemented.

3.0 ON CIRCUIT EMULATION

The On Circuit Emulation mode of operation in the 8XC51FC has not been implemented in the UT69RH051.

4.0 OPERATING CONDITIONS

The operating voltage range for the 8XC51FC is 5V ± 20%. The operating temperature range is 0° to 70°C. On the UT69RH051, the operating voltage range is 5V ± 10%. The operating temperature range is -55° to +125°C.

APPENDIX B
Impact of External Program ROM

The 8051 family of microcontrollers, including the 8XC51FC, use ports 0 and 2 to access external memory. In implementations with external program memory, these two ports are dedicated to the program ROM interface and can not be used as Input/Output ports. The UT69RH051 uses external program ROM, so ports 0 and 2 will not be available for I/O.

Military Standard Products

UT28F64 Radiation-Hardened 8K x 8 PROM

Preliminary Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

May 1994

FEATURES

- ☐ Programmable, read-only, asynchronous, radiation-hardened, 8K x 8 memory
  - Supported by industry standard programmers
- ☐ 35ns maximum address access time (-55 °C to +125 °C)
- ☐ TTL/CMOS compatible input and output levels
- ☐ Three-state data bus
- ☐ Low operating and standby current
  - Operating: 140mA maximum @28.5MHz
  - Standby: 1mA maximum (post-rad)
  - Derating: 5mA/MHz
- ☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 1.0E6 rads(Si)
  - Single event effects:
    Latchup threshold 80 MeV-cm^2/mg (min)
  - Dose rate upset: 1.0E8 rads(Si)/sec
  - Dose rate survival: 1.0E10 rads(Si)/sec
  - Neutron fluence: 1.0E14 n/cm^2
- ☐ QML Q & V compliant part (check factory for availability)
  - AC and DC testing at factory
- ☐ Packaging options:
  - 28-pin 100-mil center DIP (0.600 x 1.4)
  - 28-lead 50-mil center flatpack (0.700 x 0.75)
  - 28-lead 50-mil center flatpack (0.490 x 0.74)
- ☐ V_{DD}: 5.0 volts ± 10%

PRODUCT DESCRIPTION

The UT28F64 amorphous silicon anti-fuse PROM is a high performance, asynchronous, radiation-hardened, 8K x 8 programmable memory device. The UT28F64 PROM features fully asychronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the UT28F64. The combination of radiation-hardness, fast access time, and low power consumption make the UT28F64 ideal for high speed systems designed for operation in radiation environments.

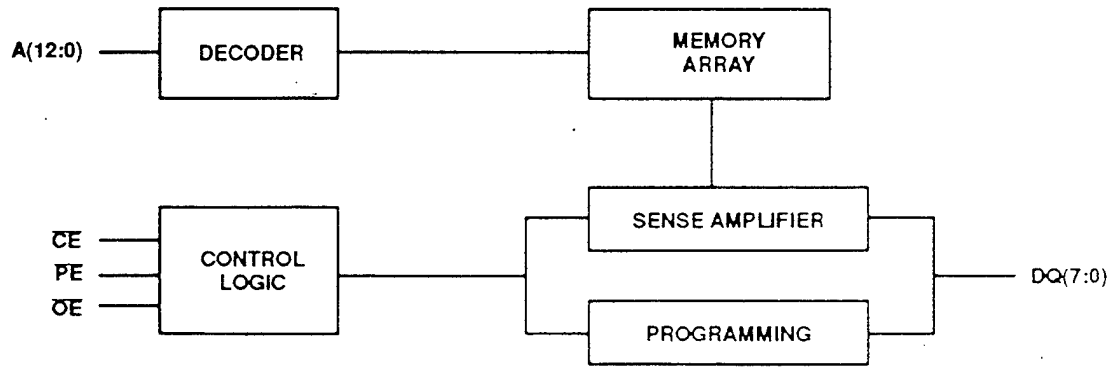
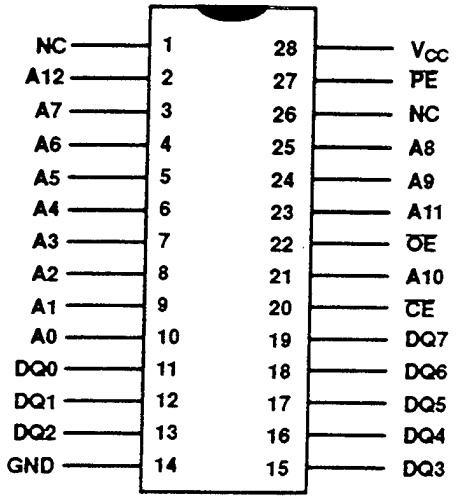


Figure 1. PROM Block Diagram

DEVICE OPERATION

The UT28F64 has three control inputs: Chip Enable ($\overline{CE}$), Program Enable ($\overline{PE}$), and Output Enable ($\overline{OE}$); thirteen address inputs, A(12:0); and eight bidirectional data lines, DQ(7:0). $\overline{CE}$ is the device enable input that controls chip selection, active, and standby modes. Asserting $\overline{CE}$ causes I_{DD} to rise to its active value and decodes the fifteen address inputs to select one of 8,192 words in the memory. $\overline{PE}$ controls program and read operations. During a read cycle, $\overline{OE}$ must be asserted to enable the outputs.

PIN CONFIGURATION



PIN NAMES

A(12:0)	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PE}$	Program Enable
DQ(7:0)	Data Input/Data Output

Table 1. Device Operation Truth Table [1]

$\overline{OE}$	$\overline{PE}$	$\overline{CE}$	I/O MODE	MODE
X	1	1	Three-state	Standby
0	1	0	Data Out	Read
1	0	0	Data In	Program
1	1	0	Three-state	Read [2]

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

ABSOLUTE MAXIMUM RATINGS [1]

(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	DC supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage on any pin	-0.5 to (V_{DD} + 0.5)	V
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation	1.5	W
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance, junction-to-case [2]	10	°C/W
I_I	DC input current	±10	mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	Positive supply voltage	4.5 to 5.5	V
T_C	Case temperature range	-55 to +125	°C
V_{IN}	DC input voltage	0 to V_{DD}	V

DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IH}	High-level input voltage	(CMOS)	3.5		V
V_{IH}	High-level input voltage	(TTL)	2.2		V
V_{IL}	Low-level input voltage	(CMOS)		1.5	V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)		V_{SS} + 0.05	V
V_{OL}	Low-level output voltage	I_{OL} = 4.0mA, V_{DD} = 4.5V (TTL)		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -200µA, V_{DD} = 4.5V (CMOS)	V_{DD} - 0.05		V
V_{OH}	High-level output voltage	I_{OH} = -400µA, V_{DD} = 4.5V (TTL)	2.4		V
C_{IN} [1]	Input capacitance	f = 1MHz @ 0V, V_{DD} = 4.5V		15	pF
C_{IO} [1]	Bidirectional I/O capacitance	f = 1MHz @ 0V, V_{DD} = 4.5V		20	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-10	10	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V $\overline{OE}$ = 5.5V	-10	10	µA
I_{OS} [2,3]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
I_{DD}(OP)[4]	Supply current operating @28.5MHz	CMOS inputs (i.e., I_{OUT} = 0) V_{DD} = 5.5V		140	mA
I_{DD}(SB) **pre-rad**	Supply current standby	CMOS inputs (i.e., I_{OUT} = 0) $\overline{CE}$ = V_{DD} - 0.5, V_{DD} = 5.5V		100	µA
I_{DD}(SB) **post-rad**	Supply current standby	CMOS inputs (i.e., I_{OUT} = 0) $\overline{CE}$ = V_{DD} - 0.5, V_{DD} = 5.5V		1	mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Guaranteed by device characterization.

READ CYCLE

A combination of $\overline{PE}$ greater than V_{IH}(min), and $\overline{CE}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data output, DQ(7:0), after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

The chip enable-controlled access is initiated by $\overline{CE}$ goir active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserte and the addresses remain stable for the entire cycle. Aft the specified t_{ELQV} is satisfied, the eight-bit word addre by A(12:0) is accessed and appears at the data outputs DQ(7:0).

Output enable-controlled access is initiated by $\overline{OE}$ going active while $\overline{CE}$ is asserted, $\overline{PE}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ELQV} have not been satisfied.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*
(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	28F64-35		28F64-45		UNIT
		MIN	MAX	MIN	MAX	
t_{AVAV}	Read cycle time	35		45		ns
t_{AVQV}	Read access time		35		45	ns
t_{AXQX}	Output hold time	0		0		ns
t_{GLQX}	$\overline{OE}$-controlled output enable time	0		0		ns
t_{GLQV}	$\overline{OE}$-controlled output enable time		15		20	ns
t_{GHQZ}	$\overline{OE}$-controlled output three-state time		15		20	ns
t_{ELQX}	$\overline{CE}$-controlled output enable time	0		0		ns
t_{ELQV}	$\overline{CE}$-controlled access time		35		45	ns
t_{EHQZ}	$\overline{CE}$-controlled output three-state time		15		20	ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

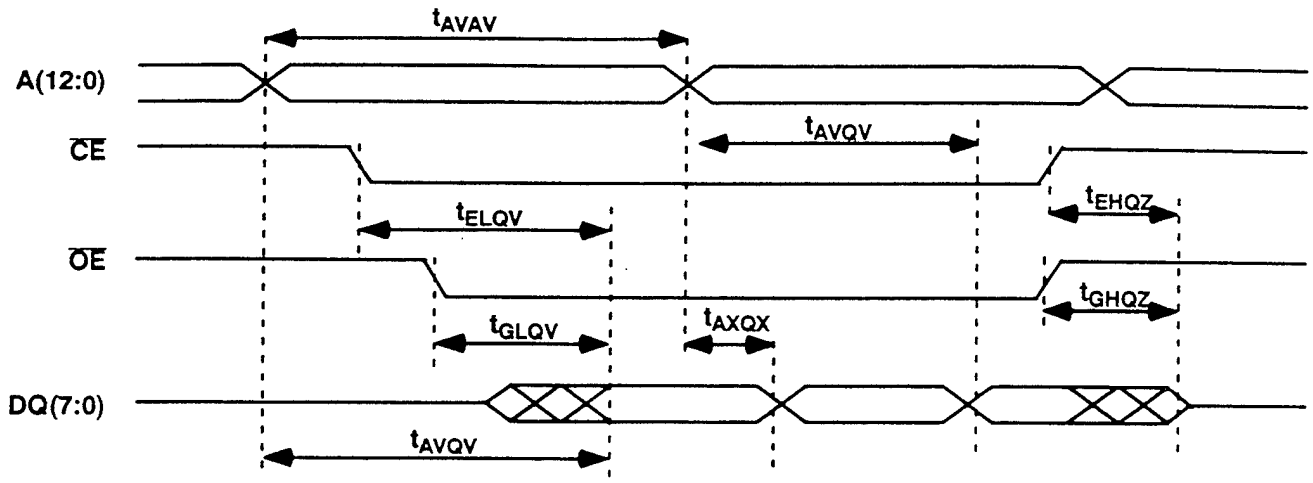


Figure 2. PROM Read Cycle

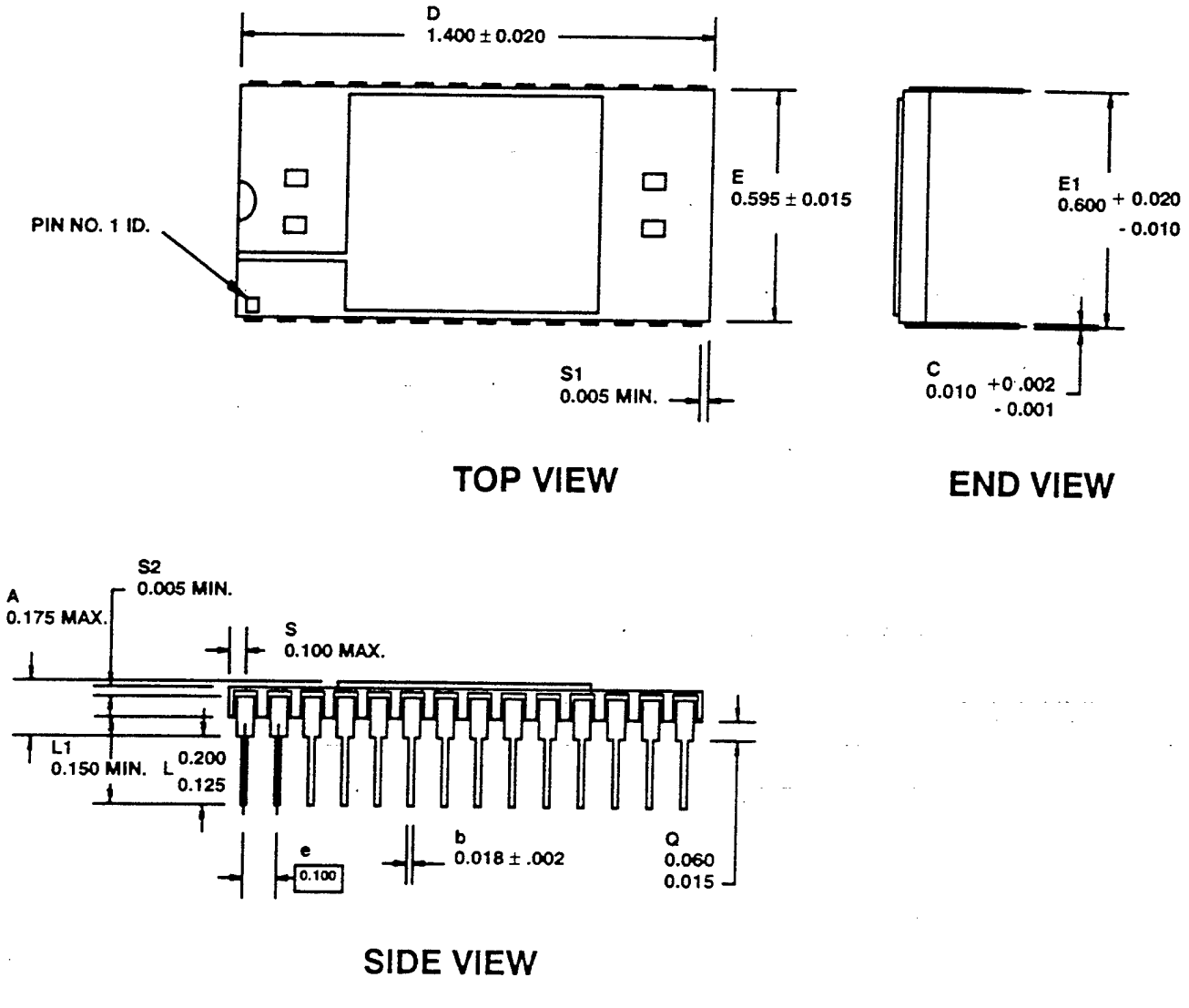
RADIATION HARDNESS

The UT28F64 PROM incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

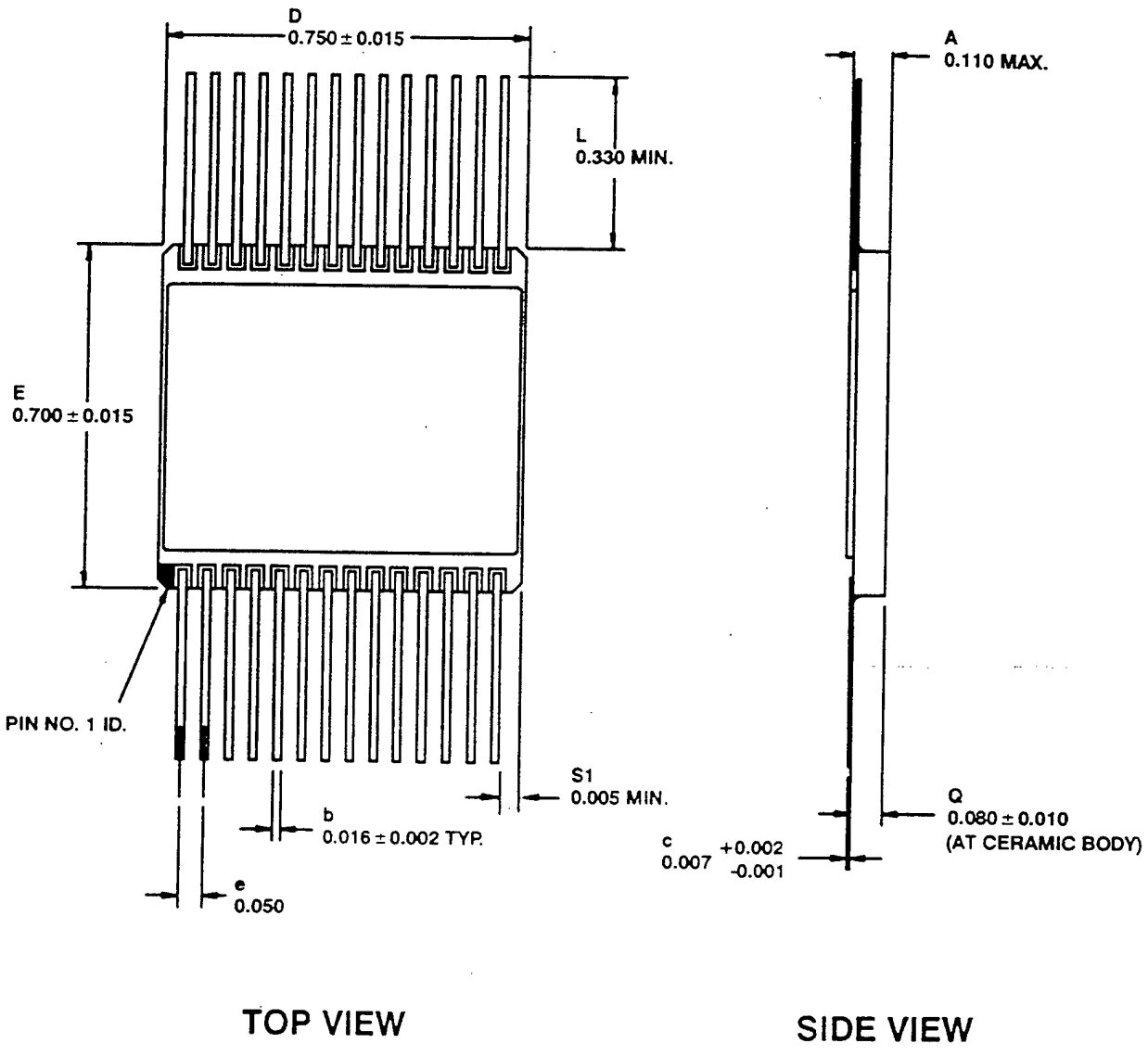
PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
Dose Rate Upset	≤ 4µs pulsewidth	1.0E8	rads(Si)/sec
Dose Rate Survival	20ns pulsewidth	1.0E10	rads(Si)/sec
LET Threshold	-55°C to +125°C	80	MeV-cm^2/mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm^2

Notes:
1. The PROM will not latchup during radiation exposure under recommended operating conditions.



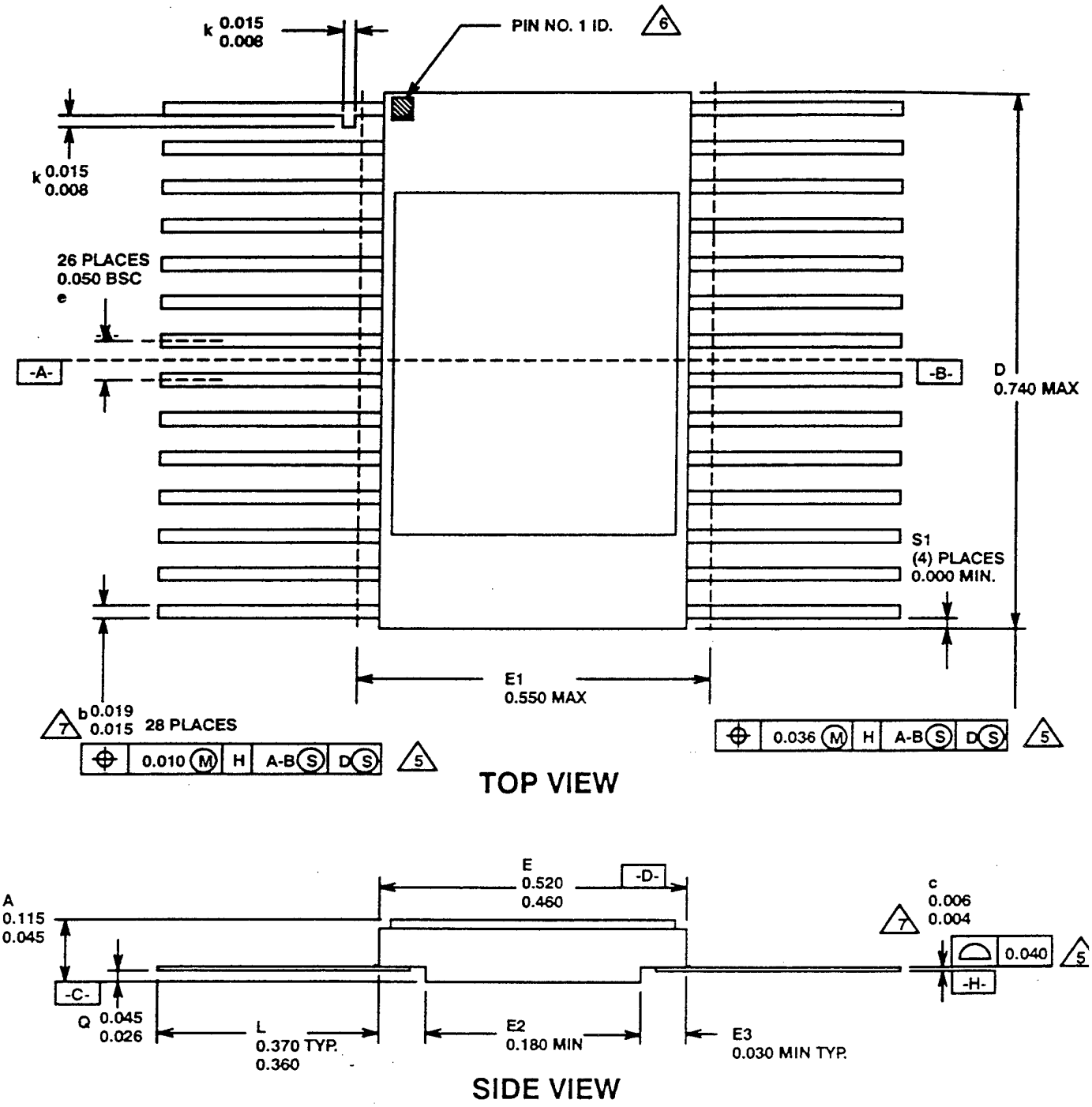
Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-I-38535.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-STD-1835.

Figure 3. 28-Pin 100-mil Center DIP (0.600 x 1.4)



Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-I-38535.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-STD-1835.

Figure 4. 28-Lead 50-mil Center Flatpack (0.700 x 0.75)



Notes:

1. All exposed metalized areas are gold plated over electroplated nickle per MIL-M-38510.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-I-38535.
4. Dimension letters refer to MIL-STD-1835.
5. Lead position and coplanarity are not measured.
6. ID mark symbol is vendor option.
7. With solder, increase maximum by 0.003.

Figure 5. 28-Lead 50-mil Center Flatpack (0.490 x 0.74)

ORDERING INFORMATION

64K PROM: Prototypes, Reduced High-Reliability, & Class S

UT 28F64 * - ** * * * *

Total Dose:
(H) = 1E6 rads(Si) per MIL-STD-883, Method 1019
(R) = 1E5 rads(Si) per MIL-STD-883, Method 1019
(5) = 1E5 rads(Si) verified with an X-ray monitor
( ) = Total dose characteristics neither tested nor guaranteed

Lead Finish: [1]
(A) = Hot solder dipped
(C) = Gold
(X) = Factory Option (gold or solder) [2]

Screening:
(S) = Class S per MIL-STD-883, Method 5004 only (QCI, per Method 5005, may be purchased separately) [3]
(V) = See note 4
(Q) = See note 4
(C) = Reduced High-Reliability flow [5]
(P) = Prototype flow [6]

Package Type:
(P) = 28-lead ceramic side-brazed DIP
(W) = 28-lead ceramic top-brazed flatpack (0.050" lead pitch; 0.700" x 0.750" body)
(X) = 28-lead ceramic bottom-brazed flatpack (0.050" lead pitch; 0.490" x 0.740" body)

Access Time:
(35) = 35ns access time
(45) = 45ns access time

Device Type Modifier:
(T) = TTL-compatible I/O levels
(C) = CMOS-compatible I/O levels

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose must be specified. (Not available without radiation hardening.)
4. This device will be offered as a MIL-I-38535 QML Q, QML V, or SMD device. Anticipated availability is 3Q94. Please contact UTMC for the correct part number and ordering information.
5. Reduced High-Reliability flow per *UTMC Manufacturing Flows Technical Description*. Devices have 48 hours of burn-in and are tested at -55°C, room temperature, and 125°C. Radiation characteristics are neither tested nor guaranteed and may not be specified.
6. Prototype flow per *UTMC Manufacturing Flows Technical Description*. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is at UTMC's option and an "X" must be specified when ordering.

Military-Standard Products

UT67164 Radiation-Hardened 8K x 8 SRAM -- SEU Hard

Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

February 1992

FEATURES

- ☐ 55ns maximum address access time, single-event upset less than 1.0E-10 errors/bit-day (-55°C to +125°C)
- ☐ Asynchronous operation for compatibility with industry-standard 8K x 8 SRAM
- ☐ TTL-compatible input and output levels
- ☐ Three-state bidirectional data bus
- ☐ Low operating and standby current
- ☐ Full military operating temperature range, -55°C to +125°C, screened to specific test methods listed in Table I MIL-STD-883 Method 5004 for Class S or Class B
- ☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0E6 rads (Si)
  - Dose rate upset: 1.0E9 rads (Si)/sec
  - Dose rate survival: 1.0E12 rads (Si)/sec
  - Single-event upset: <1.0E-10 errors/bit-day
- ☐ Industry standard (JEDEC) 64K SRAM pinout
- ☐ Packaging options:
  - 28-pin 100-mil center DIP (.600 x 1.2)
  - 28-pin 50-mil center flatpack (.700 x .75)
- ☐ 5-volt operation
- ☐ Post-radiation AC/DC performance characteristics guaranteed by MIL-STD-883 Method 1019 testing at 1.0E6 rads(Si)

INTRODUCTION

The UT67164 SRAM is a high performance, asynchronous, radiation-hardened, 8K x 8 random access memory conforming to industry-standard fit, form, and function. The UT67164 SRAM features fully static operation requiring no external clocks or timing strobes. UTMC designed and implemented the UT67164 SRAM using an advanced radiation-hardened twin-well CMOS process. Advanced CMOS processing along with a device enable/disable function result in a high performance, power-saving SRAM. The combination of radiation-hardness, fast access time, and low power consumption make UT67164 ideal for high-speed systems designed for operation in radiation environments.

PIN NAMES

A(12:0)	Address	$\overline{W}$	Write
DQ(7:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{E1}$	Enable 1	V_{DD}	Power
E2	Enable 2	V_{SS}	Ground

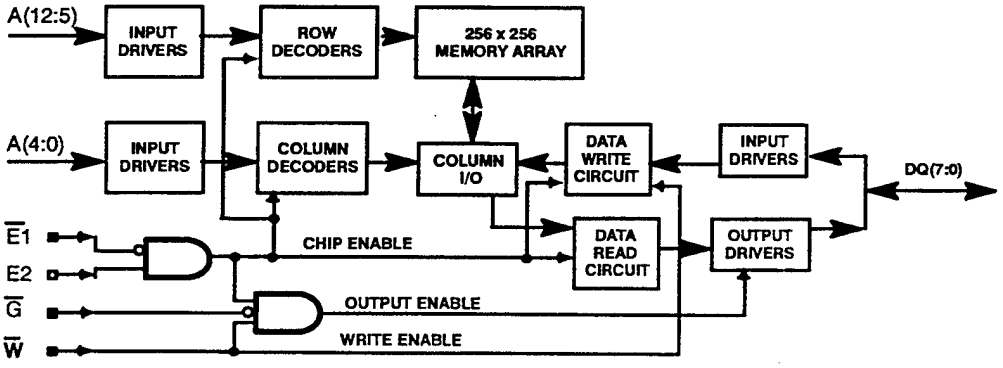


Figure 1. SRAM Block Diagram

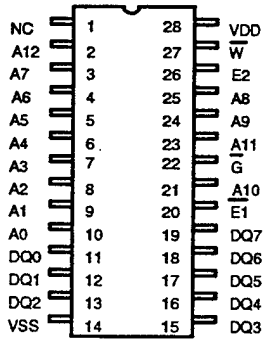


Figure 2. SRAM Pinout

DEVICE OPERATION

The UT67164 has four control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); thirteen address inputs, A(12:0); and eight bidirectional data lines, DQ(7:0). $\overline{E1}$ and E2 are device enable inputs that control device selection, active, and standby modes. Asserting both $\overline{E1}$ and E2 enables the device, causes IDD to rise to its active value, and decodes the thirteen address inputs to select one of 8,192 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	$\overline{E1}$	E2	I/O Mode	Mode
X [1]	X	X	0	3-state	Stand-by
X	X	1	X	3-state	Stand-by
X	0	0	1	Data in	Write
1	1	0	1	3-state	Read [2]
0	1	0	1	Data out	Read

Notes:
1. "X" is defined as a "don't care" condition.
2. Device active; outputs disabled.

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH}(min), $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a read cycle. Read access time is measured from the latter of device enable, Output Enable, or valid address to valid data output.

Read Cycle 1, the Address Access read in figure 3a, is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Figure 3b shows Read Cycle 2, the Chip Enable-controlled Access. For this cycle, $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the eight-bit word addressed by A(12:0) is accessed and appears at the data outputs DQ(7:0).

Figure 3c shows Read Cycle 3, the Output Enable-controlled Access. For this cycle, $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable before $\overline{G}$ is enabled. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ less than V_{IL}(max), $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when W is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access shown in figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by the latter of $\overline{E1}$ or E2. Unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access shown in figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by the latter of $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ(7:0) to avoid bus contention.

RADIATION HARDNESS

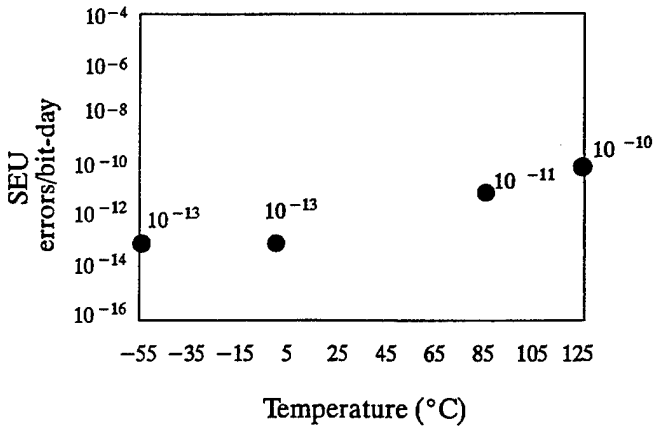
The UT67164 SRAM incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

Table 2. Radiation Hardness Design Specifications [1]

Total Dose	1.0E6	rads(Si)
Dose Rate Upset	1.0E9	rads(Si)/s 20ns pulse
Dose Rate Survival	1.0E12	rads(Si)/s 20ns pulse
Single-Event Upset	1.0E-10	errors/bit-day [2]
Neutron Fluence	3.0E14	n/cm2

Notes:
1. The SRAM will not latch up during radiation exposure under recommended operating conditions.
2. 90% Adam's worst case spectrum (-55°C to +125°C).

Table 3. SEU versus Temperature



ABSOLUTE MAXIMUM RATINGS [1] (Referenced to Vss)

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.5 to 7.0
$V_{I/O}$	Voltage on any pin	-0.5 to V_{DD} + 0.5
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.0 W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case [2]	10°C/W
I_{LU}	Latchup immunity (see figure 6b)	+/- 150 mA
I_I	DC input current	+/- 10 mA

Notes:
1.. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	Positive supply voltage	4.5 to 5.5	V
T_C	Case temperature range	-55 to +125	°C
V_{IN}	DC input voltage	0 to V_{DD}	V

DC ELECTRICAL CHARACTERISTICS (Post-Radiation)*
(V_{DD} = 5.0V +/-10%; -55°C < Tc < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IH}	High-level input voltage		2.2		V
V_{IL}	Low-level input voltage			0.8	V
V_{OL}	Low-level output voltage	I_{OL} = +/- 4.0 mA, V_{DD} = 4.5V		0.4	V
V_{OH}	High-level output voltage	I_{OH} = +/- 4.0mA, V_{DD} = 4.5V	2.4		V
C_{IN}	Input capacitance [1]	F = 1MHz @ 0V, V_{DD} = 4.5V		15	pF
C_O	Bidirectional I/O capacitance [1]	F = 1MHz @ 0V, V_{DD} = 4.5V		20	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-10	10	µA
I_{OZ}	Three-state output leakage current TTL outputs	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V $\overline{G}$ = 5.5V	-10	10	µA
I_{OS}	Short-circuit output current [2,3]	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
I_{DD}(OP)	Supply current operating @1MHz	CMOS inputs (i.e., I_{OUT} = 0) V_{DD} = 5.5V		40	mA
I_{DD}(SB) pre-rad	Supply current standby	CMOS inputs (i.e., I_{OUT} = 0) $\overline{E1}$ = V_{DD} - 0.5 V_{DD} = 5.5V E2 = V_{SS} + 0.5		200	µA
I_{DD}(SB) post-rad	Supply current standby @ f = 0Hz	CMOS inputs (i.e., I_{OUT} = 0) CS1 = negated V_{DD} = 5.5 V CS2 = negated		3	mA

Notes:
1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

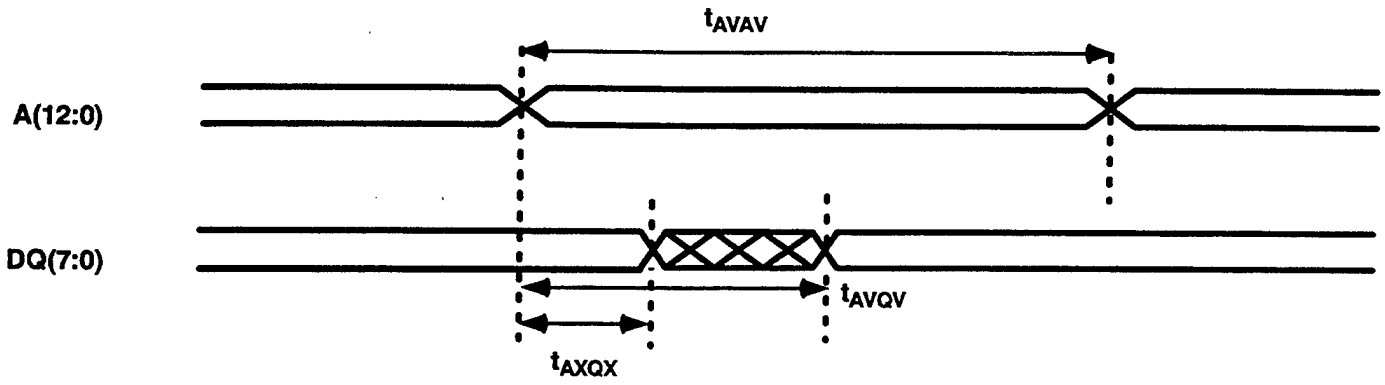
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*
(V_{DD} = 5.0V +/-10%; -55°C < Tc < +125°C)

SYMBOL	PARAMETER	67164-85		67164-70		67164-55		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Read cycle time	85		70		55		ns
t_{AVQV}	Read access time		85		70		55	ns
t_{AXQX}	Output hold time	5		5		5		ns
t_{GLQX}	$\overline{G}$-controlled output enable time	0		0		0		ns
t_{GLQV}	$\overline{G}$-controlled output enable time (Read Cycle 3)		30		15		15	ns
t_{GHQZ}	$\overline{G}$-controlled output three-state time		15		15		15	ns
t_{ETQX} [1]	E-controlled output enable time	0		0		0		ns
t_{ETQV} [1]	E-controlled access time		85		70		55	ns
t_{EFQZ} [2]	E-controlled output three-state time [3]		25		20		20	ns

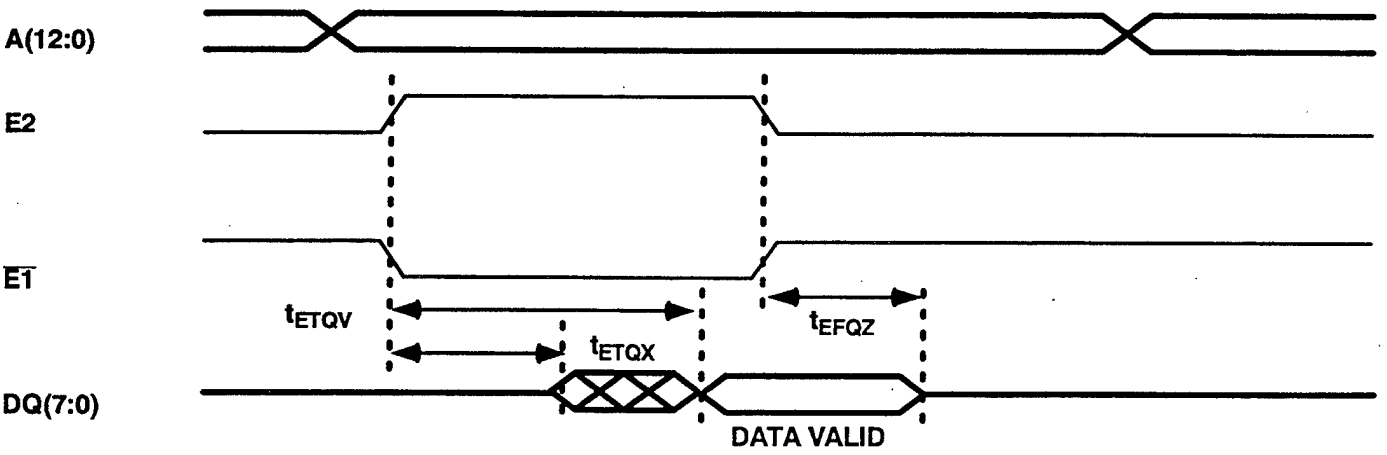
Notes:
1. The ET (enable true) notation refers to the rising edge of E2 or the falling edge of $\overline{E1}$, whichever comes last. SEU immunity does not affect the read parameters.
2. The EF (enable false) notation refers to the falling edge of E2 or the rising edge of $\overline{E1}$, whichever comes first. SEU immunity does not affect the read parameters.
3. Three-state is defined as a 500mV change from steady-state output voltage.

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).



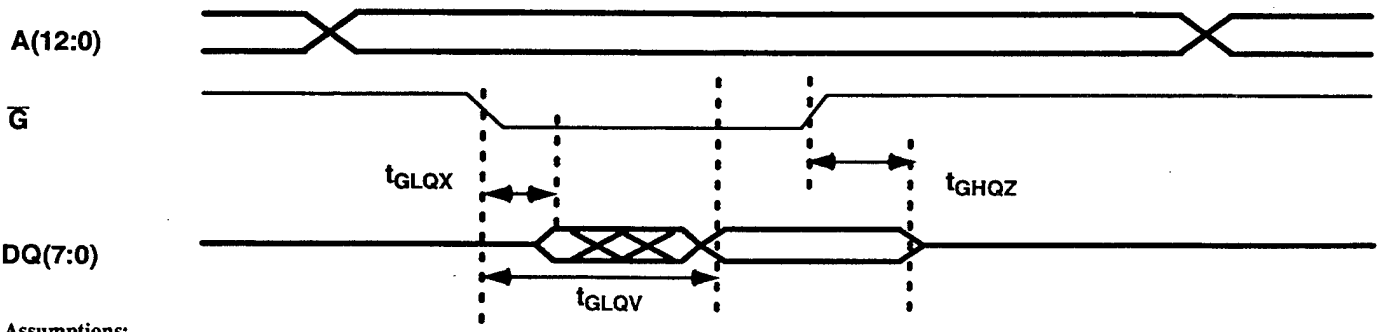
Assumptions:
1. $\overline{E1}$ and $\overline{G} \leq V_{IL}$ (max)
2. E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $G \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



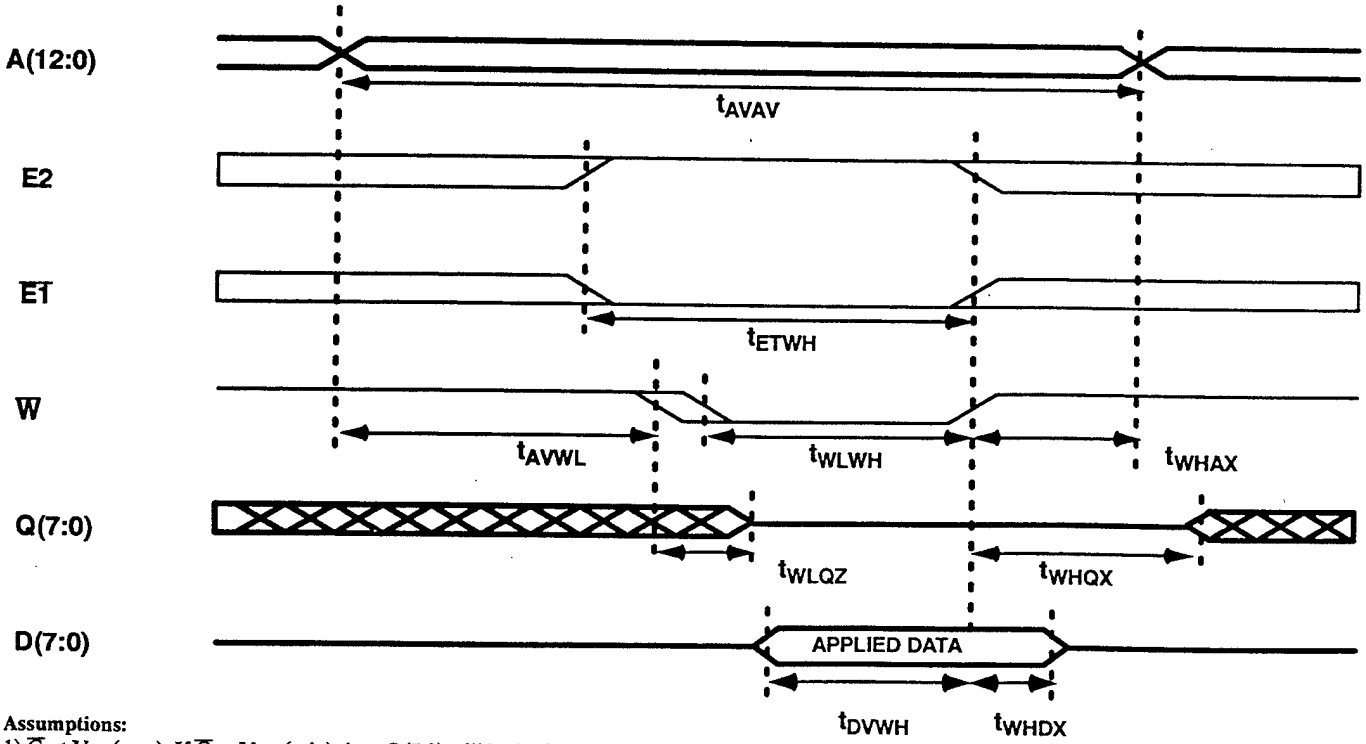
Assumptions:
1. $\overline{E1} \leq V_{IL}$ (max)
2. E2 and $\overline{W} \geq V_{IH}$ (min)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

AC CHARACTERISTICS WRITE CYCLE (Post-Radiation)*
(V_{DD} = 5.0V +/-10%; -55°C < Tc < +125°C)

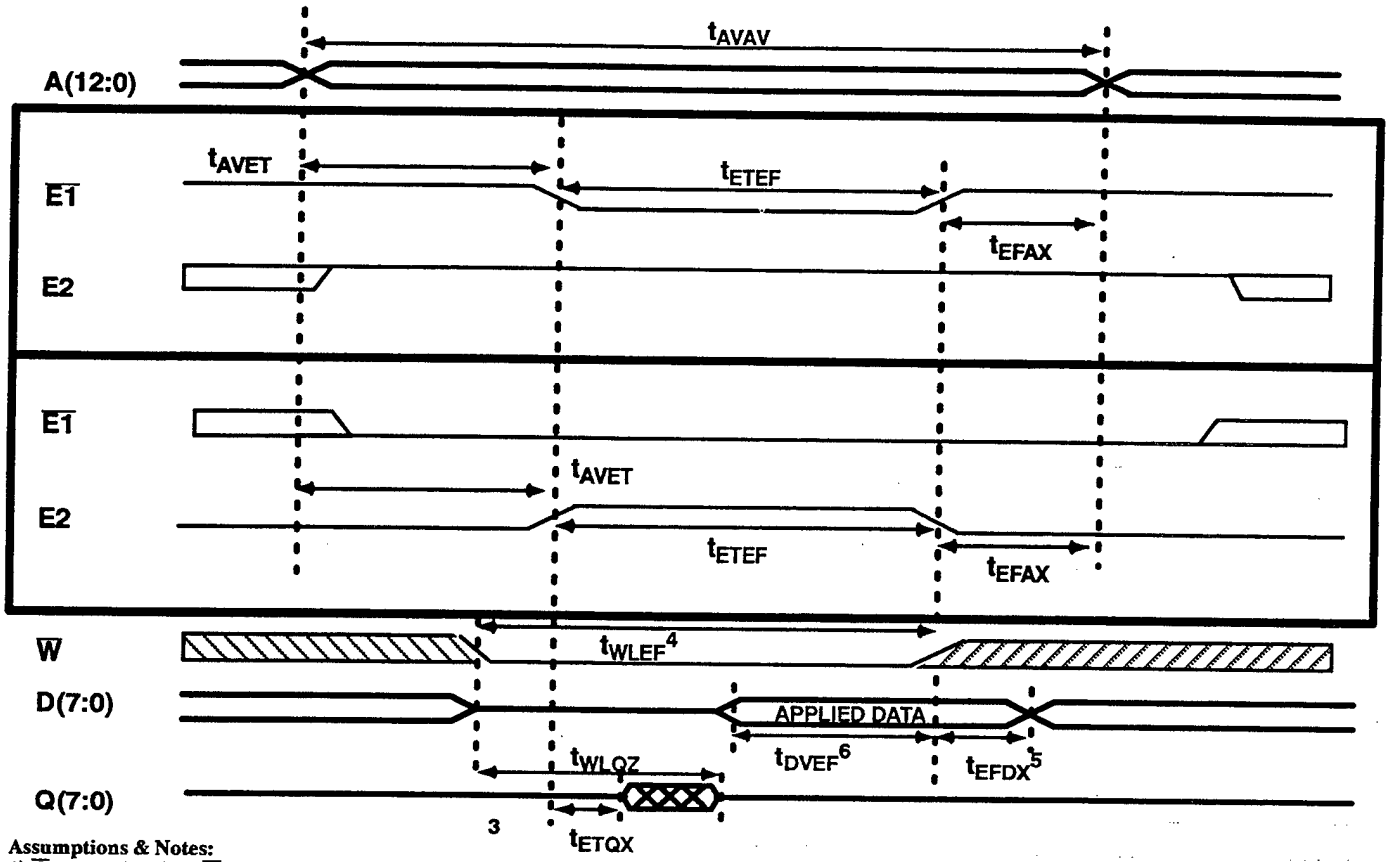
SYMBOL	PARAMETER	67164-85		67164-70		67164-55		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVAV}	Write cycle time	85		70		55		ns
t_{ETWH}	Device enable to end of write	65		60		50		ns
t_{AVET}	Address setup time for write ($\overline{E1}$ or E2 - controlled)	0		0		0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		0		0		ns
t_{WLWH}	Write pulse width	50		35		35		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		0		0		ns
t_{EFAX}	Address hold time for device enable ($\overline{E1}$ or E2 - controlled)	0		0		0		ns
t_{WLQZ}	$\overline{W}$-controlled three-state time		15		15		15	ns
t_{WHQX}	$\overline{W}$-controlled output enable time	0		0		0		ns
t_{ETEF}	Device enable pulse width ($\overline{E1}$ or E2 - controlled)	65		60		50		ns
t_{DVWH}	Data setup time	50		35		35		ns
t_{WHDX}	Data hold time	0		0		0		ns
t_{WLEF}	Device enable controlled write pulse width	65		60		50		ns
t_{DVEF}	Data setup time	50		35		35		ns
t_{EFDX}	Data hold time	0		0		0		ns

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).



Assumptions:
1) $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.

Figure 4a. SRAM Write Cycle 1: $\overline{W}$-Controlled Access



Assumptions & Notes:

1) $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(7:0) will be in three-state for the entire cycle.
2) Either $\overline{E1}$/E2 scenario above can occur.
3) If $\overline{E1}$ or E2 is asserted simultaneously with or after the $\overline{W}$ low transition, the outputs will remain in a high-impedance state.
4) $t_{WLEF} = t_{ETWH}$
5) $t_{EFDX} = t_{WHDX}$
6) $t_{DVEF} = t_{DVWH}$

Figure 4b. SRAM Write Cycle 2: Enable-Controlled Access

DATA RETENTION CHARACTERISTICS (Post-Radiation)*
(T_C = 25°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM V_{DD} @ 2.0V	MAXIMUM V_{DD} @ 3.0V	UNIT
V_{DR}	V_{DD} for data retention	2.0	--	--	V
I_{DDDR}	Data retention current [1]	--	75	90	µA
t_{EFR}	Chip deselect to data retention time [1]	0			ns
t_R	Operation recovery time [1]	t_{AVAV}			ns

Note::
1. V_{LC} = 0.2V
   V_{HC} = V_{DD} -0.2V
   $\overline{E1} \geq V_{HC}$, E2 > V_{HC}

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

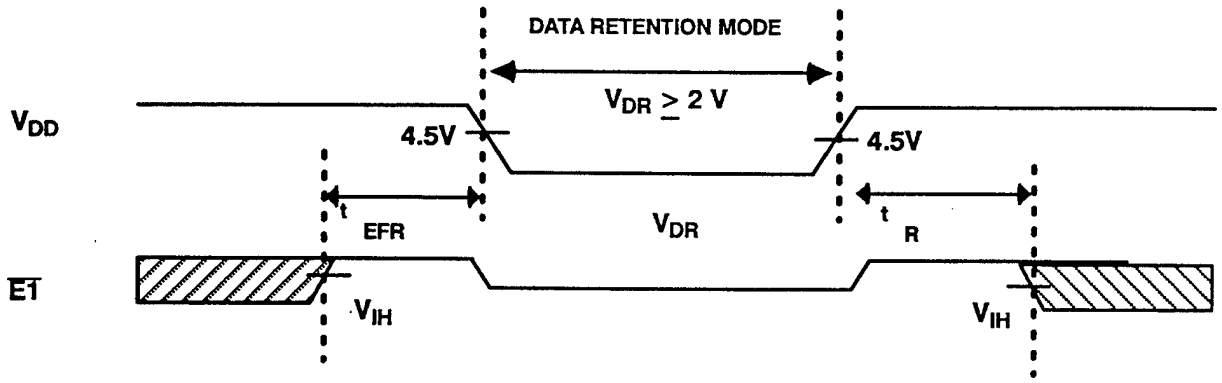
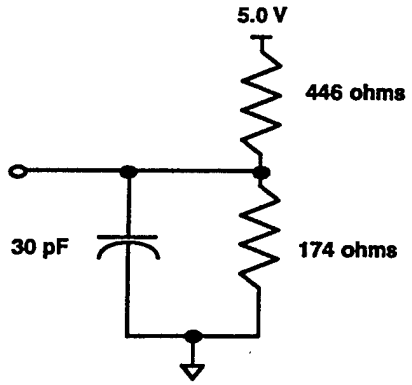
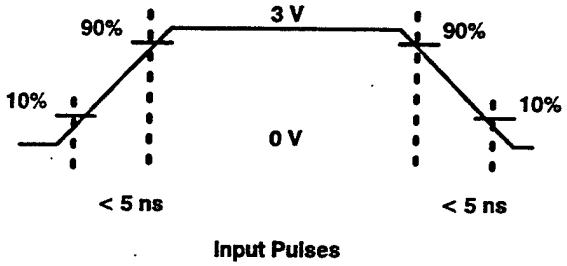


Figure 5. Low V_{DD} Data Retention Waveform





Assumptions:
1. 30 pF including scope probe and test socket.
2. Measurement of data output occurs at the low to high or high to low transition mid-point.

Figure 6a. AC Test Loads and Input Waveforms

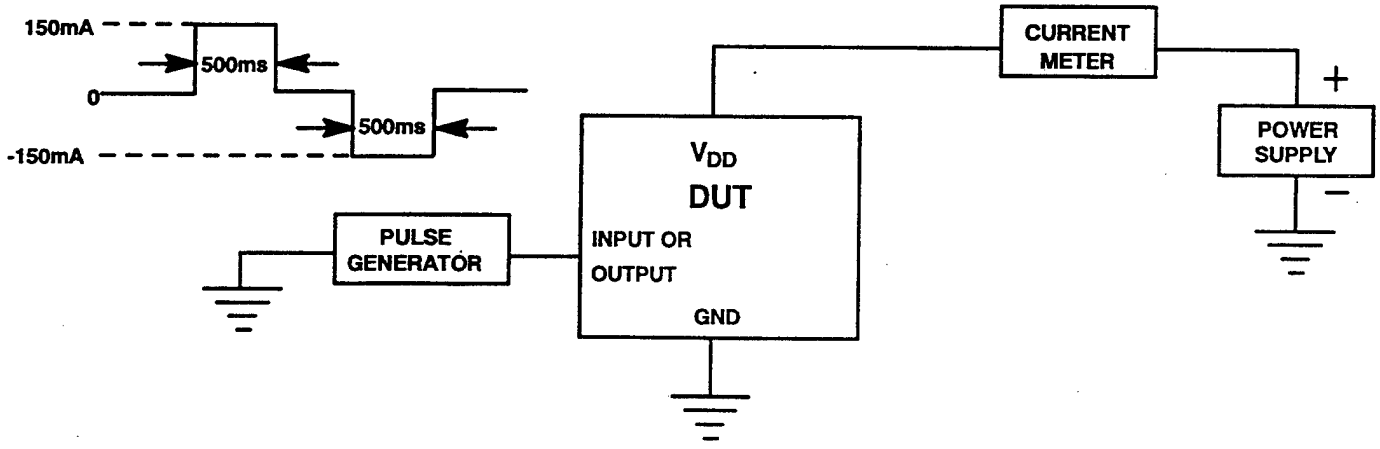
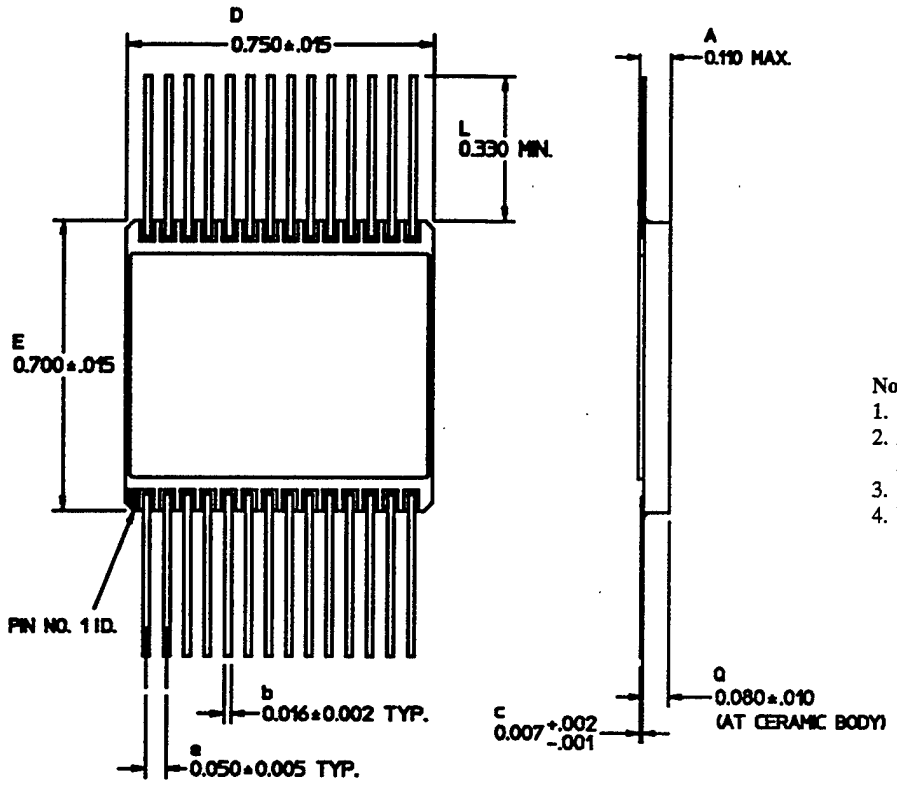


Figure 6b. Latchup Test

LATCHUP TEST CONFIGURATION

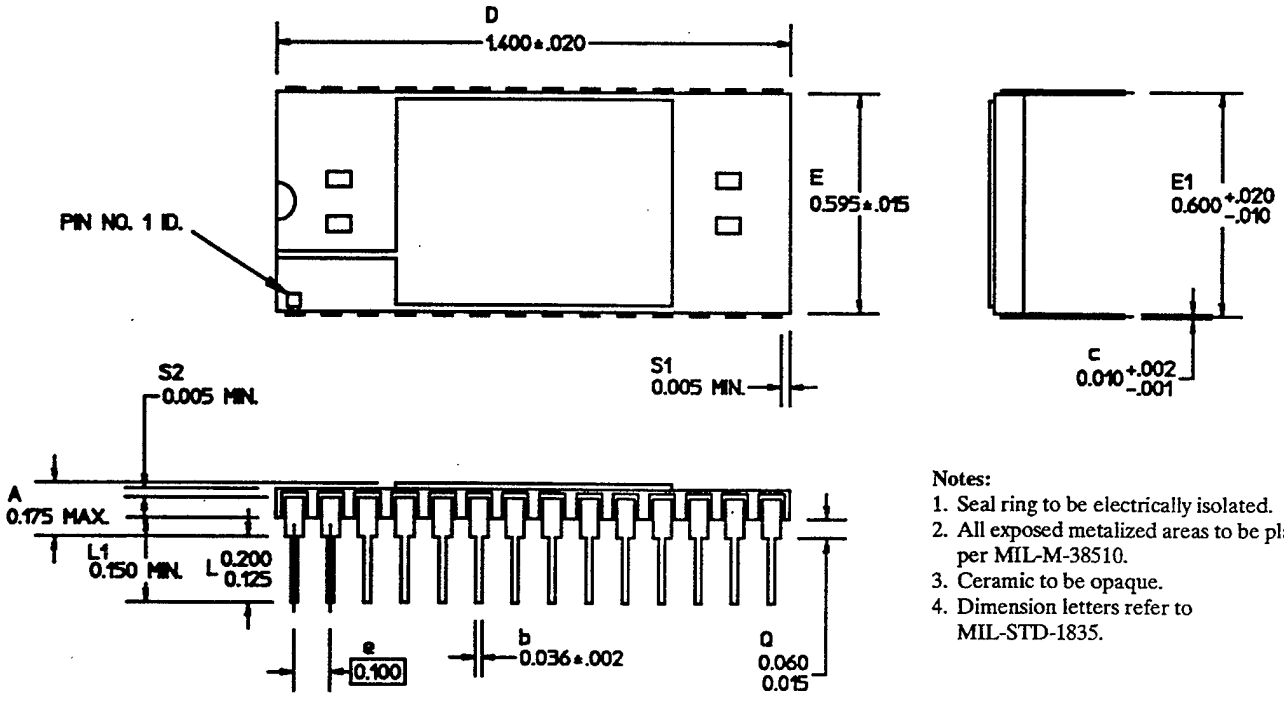
Figure 6b shows the latchup test. V_{DD} holds at +5.5 V_{DC}, and V_{SS} holds at ground. The device test is at 125°C. Each type of I/O alternately receives a positive and then negative 150 mA pulse of 500 ms duration. The current is monitored after the pulse for latchup condition. To prevent burnout, the supply current is limited to 400 mA.

The SRAM has latchup immunity in excess of +150 mA for 500 ms.



Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-M-38510.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-STD-1835.

Figure 7a. 28-pin Ceramic Flatpack



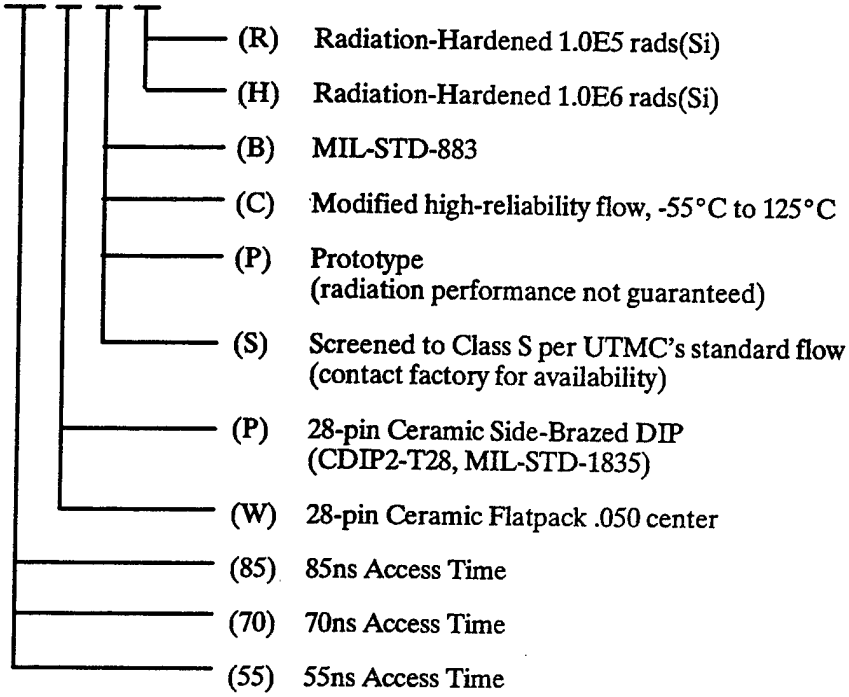
Notes:
1. Seal ring to be electrically isolated.
2. All exposed metalized areas to be plated per MIL-M-38510.
3. Ceramic to be opaque.
4. Dimension letters refer to MIL-STD-1835.

Figure 7b. 28-pin Ceramic DIP Package

ORDERING INFORMATION

To order the UT67164 SRAM, use the following part number guide:

UT67164 ** * * *



MAXIM

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

General Description

The MAX220-MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, and in particular, for those applications where ±12V is not available.

These parts are particulary useful in battery-powered systems since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225 MAX233, MAX235, and MAX245-MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

Superior to Bipolar

- Operate from Single +5V Power Supply (+5V and +12V—MAX231 and MAX239)
- Low-Power Receive Mode in Shutdown (MAX223/MAX242)
- Meet All EIA/TIA-232E and V.28 Specifications
- Multiple Drivers and Receivers
- 3-State Driver and Receiver Outputs
- Open-Line Detection (MAX243)

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

Contact factory for dice specifications

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	4.7/10			120	Low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1			200	+5V, 8kV ESD-protected, serial mouse drivers with 0.1µF charge-pump capacitors
MAX223 (MAX213)	+5	4/5	4	1.0/0.1	•	✓	120	MAX241 without shutdown mode
MAX225	+5	5/5	0		•	✓	120	Available in SO
MAX226 (MAX206)	+5	5/5	4	1.0/0.1				5 drivers with shutdown
MAX231 (MAX201)	+5 and +12	2/2	4	1.0/0.1				Standard +5V/+12V RS-232 interface (replaces MAX232)
	+5 and +12 to +15							Improved MAX232
MAX232 (MAX202)	+5	2/2	4	1.0/0.1			120	Industry standard
MAX232A	+5	2/2	4	0.1			200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0				120	No external caps
MAX233A	+5	2/2	0				200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0/0.1			120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0		•		120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0/0.1	•		120	Shutdown, three-state
MAX237 (MAX207)	+5	5/3	4	1.0/0.1	•		120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0/0.1	•		120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3/5	4	1.0/0.1	•		120	Standard +5V/+12V or battery-supplied RS-232
								Package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	•		120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0/0.1	•		120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	•	✓	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	•		120	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	•		120	High slew rate
MAX245	+5	8/10	0		•	✓	120	High slew rate, int. caps, too (MAX220 pinout)
MAX246	+5	8/10	0		•	✓	120	High slew rate, int. caps, three-state shutdown modes
MAX247	+5	8/9	0		•	✓	120	High slew rate, int. caps, inverting receivers
MAX248	+5	8/8	4	1.0	•	✓	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	•	✓	120	Available in quad flatpack package

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
T_{OUT} (Note 1) ..... ±15V
Output Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Driver/Receiver Output Short Circuited to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) 800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _ ..... 0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ ..... -40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Normal operation			5	40	µA
	$\overline{SHDN}$ = 0V, MAX222-242, shutdown			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate	Except MAX220, normal operation			200	116	kbits/sec
	MAX220			22	20	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V			±7	±22	mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	Except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	Except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	Except MAX243, V_{CC} = 5V, no hyst. in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243 (continued)

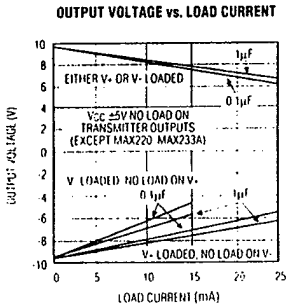
(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

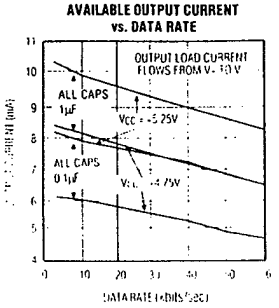
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{EN}$ Input Threshold Low	MAX242			1.4	0.8	V
$\overline{EN}$ Input Threshold High	MAX242		2.0	1.4		V
POWER SUPPLY						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5, 6, 9, 19	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both outputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current	MAX222/242				±1	µA
$\overline{SHDN}$ Threshold Low	MAX222/242			1.4	0.8	V
$\overline{SHDN}$ Threshold High	MAX222/242		2.0	1.4		V
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TTL to RS-232 (Normal Operation) Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	1	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TTL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX242		160	500	
Transmitter-Output Enable Time ($\overline{SHDN}$ goes High), Figure 4	t_{ET}	MAX222/242, 1µF caps (includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes Low), Figure 4	t_{DT}	MAX222/242, 1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLR} - t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

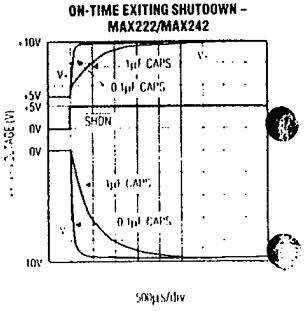
Note 2: MAX243 $R2_{OUT}$ is guaranteed to be low when $R2_{IN}$ ≥ 0V or is floating.

Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243







ABSOLUTE MAXIMUM RATINGS—MAX223/MAX230-MAX241

V_{CC} ..... -0.3V to +6V
$V+$ ..... (V_{CC} - 0.3V) to +14V
$V-$ ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ... 800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) ... 889mW
24-Pin Narrow Plastic DIP (derate 13.33mW/°C above +70°C) ... 1067mW
24-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 500mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ... 800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) ... 941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ... 1000mW
44-Pin Plastic FP (derate 11.11mW/°C above +70°C) ... 889mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) ... 727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) ... 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) ... 889mW
24-Pin Narrow CERDIP (derate 12.50mW/°C above +70°C) ... 1000mW
24-Pin Sidebraze (derate 20.0mW/°C above +70°C) ... 1600mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) ... 762mW
Operating Temperature Ranges
MAX2__C__ ..... 0°C to +70°C
MAX2__E__ ..... -40°C to +85°C
MAX2__M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX223/MAX230-MAX241

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 30kΩ to ground		±5.0	±7.3		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX232/233		5	10	mA
		MAX223/232,230/234-238/240/241		7	15	
		MAX231-239		4	8	
V+ Power-Supply Current		MAX231		1.8	5	mA
		MAX234		5	10	
Shutdown Supply Current	T_A = +25°C	MAX223		15	50	µA
		MAX230-235/240/241		1	10	
Input Logic Threshold Low	T_{IN}, EN, SHDN (MAX223); EN, SHDN (MAX230/235-241)				1.8	V
Input Logic Threshold High	T_{IN}		2.0			V
	EN, SHDN (MAX223); EN, SHDN (MAX230/235-241)		2.4			
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
Receiver Input Voltage Operating Range			-30		+30	V

ELECTRICAL CHARACTERISTICS — MAX223/MAX230-MAX241 (continued)

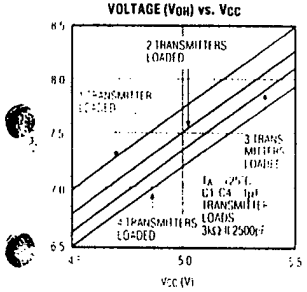
(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)			0.8	1.2	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V ($R4_{IN}$, $R5_{IN}$)			0.6	1.5	
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal operation $\overline{SHDN}$ = 5V (MAX223) SHDN = 0V (MAX235/236/240/241)			1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V ($R4_{IN}$, $R5_{IN}$)			1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V, no hysteresis in shutdown			0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233 I_{OUT} = 3.2mA)					0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = 1.0mA			3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX235-241)				0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223			600		ns
		MAX235/236/239/240/241			400		
Receiver Output Disable Time	Normal operation	MAX223			900		ns
		MAX235/236/239/240/241			250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF	Normal operation			0.5	10	µs
		$\overline{SHDN}$ = 0V (MAX223)	tPHLS		4	40	
			tPLHS		6	40	
Transition Region Slew Rate	MAX223/MAX230/MAX234-241 T_A = +25°C, V_{CC} = 5V R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF measured from +3V to -3V or -3V to +3V			3	5.1	30	V/µs
	MAX231/MAX232/MAX233 T_A = +25°C, V_{CC} = 5V R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF measured from +3V to -3V or -3V to +3V				4	30	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V			300			Ω
Transmitter Out Short-Circuit Current					±10		mA

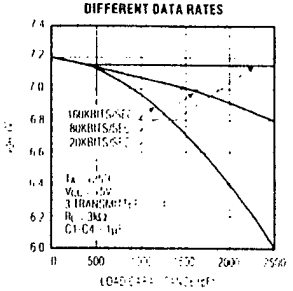
Typical Operating Characteristics

MAX223/MAX230/MAX234-241

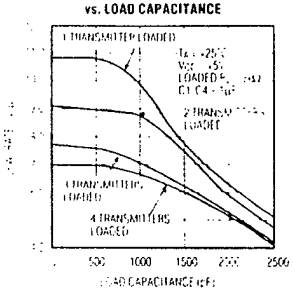
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



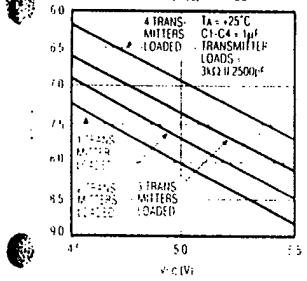
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



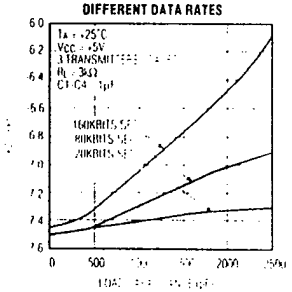
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



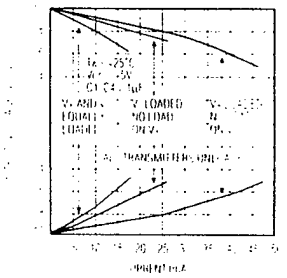
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



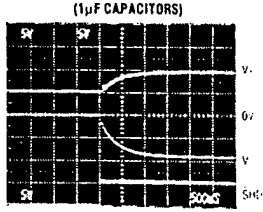
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE V+, V- vs. LOAD CURRENT



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY REVERSED FOR THE MAX241

ABSOLUTE MAXIMUM RATINGS—MAX225/MAX244-MAX249

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN}, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENR}$, $\overline{ENT}$, $\overline{ENRA}$, $\overline{ENRB}$, $\overline{ENTA}$, $\overline{ENTB}$ ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±25V
T_{OUT} (Note 3) ..... ±15V
R_{OUT} ..... -0.3V to (VCC + 0.3V)
Short Circuit (1 output at a time)
T_{OUT} to GND ..... Continuous
R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin Wide SO (derate 12.50mW/°C above +70°C) 1000mW
40-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 611mW
44-Pin PLCC (derate 13.33mW/°C above +70°C) 1067mW
Operating Temperature Ranges:
MAX225C_ _, MAX24_C_ _ ..... 0°C to +70°C
MAX225E_ _, MAX24_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 3: Input Voltage measured with transmitter output in a high-impedance state, shutdown, or V_{CC} = 0V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX225/MAX244-MAX249

(MAX225 V_{CC} = 5.0V ±5%; MAX244-MAX249 V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Tables 1A-1D	Normal operation		10	50	µA
		Shutdown		±0.01	±1	
Data Rate	Tables 1A-1D, Normal operation			120	64	kbits/sec
Output Voltage Swing	All transmitter outputs loaded with 3Ωk to GND		±5	±7.5		V
Output Leakage Current (Shutdown)	Tables 1A-1D	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENT}$, $\overline{ENTA}$, $\overline{ENTB}$ = V_{CC}, V_{OUT} = ±15V		±0.01	±25	µA
		V_{CC} = 0V, V_{OUT} = ±15V		±0.01	±25	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 4)		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V			±7	±30	mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±25	V
RS-232 Input Threshold Low	V_{CC} = 5V		0.8	1.3		V
RS-232 Input Threshold High	V_{CC} = 5V			1.8	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled, Tables 1A-1D, 0V ≤ V_{OUT} ≤ V_{CC}, $\overline{ENR}$_ = V_{CC}			±0.05	±0.10	µA

ELECTRICAL CHARACTERISTICS—MAX225/MAX244-MAX249 (continued)

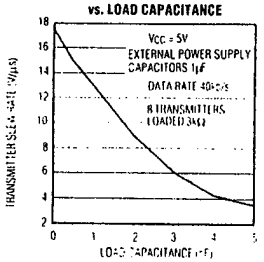
(MAX225 V_{CC} = 5.0V ±5%, MAX244-MAX249 V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

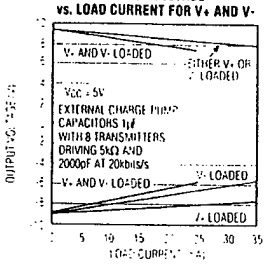
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC						
Operating Supply Voltage		MAX225	4.75		5.25	V
		MAX244-MAX249	4.5		5.5	
V_{CC} Supply Current (Normal Operation)	No Load	MAX225		10	20	mA
		MAX244-MAX249		11	30	
	3kΩ loads on all outputs	MAX225		40		
		MAX244-MAX249		57		
Shutdown Supply Current	T_A = +25°C			8	25	µA
	T_A = T_{MIN} to T_{MAX}				50	
Control Input	Leakage Current				±1	µA
	Threshold Low			1.4	0.8	V
	Threshold High		2.4	1.4		
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V		5	10	30	V/µs
Transmitter Propagation Delay TTL to RS-232 (Normal Operation) Figure 1	t_{PHL}			1.3	3.5	µs
	t_{PLH}			1.5	3.5	
Receiver Propagation Delay TTL to RS-232 (Normal Operation) Figure 2	t_{PHLR}			0.6	1.5	µs
	t_{PLHR}			0.6	1.5	
Receiver Propagation Delay TTL to RS-232 (Low Power Mode) Figure 2	t_{PHLS}			0.6	10	µs
	t_{PLHS}			3.0	10	
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHL} - t_{PLH}			350		ns
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHL} - t_{PLH}			350		ns
Receiver-Output Enable Time, Figure 3	t_{ER}			100	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}			100	500	ns
Transmitter Enable Time	t_{ET}	MAX246-249 (excludes charge-pump startup)		6		µs
		MAX225/MAX245-MAX249 (includes charge-pump startup)		10		ms
Transmitter Disable Time, Figure 4	t_{DT}			100		ns

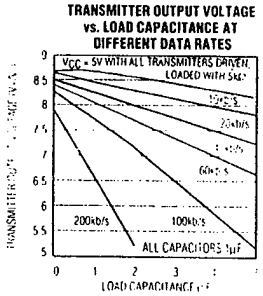
Note 4: The 300Ω minimum specification complies with EIA/TIA-232E, but the actual resistance when in shutdown mode or V_{CC} = 0 is 10MΩ as is implied by the leakage specification.

Typical Operating Characteristics

MAX225/MAX244-MAX249







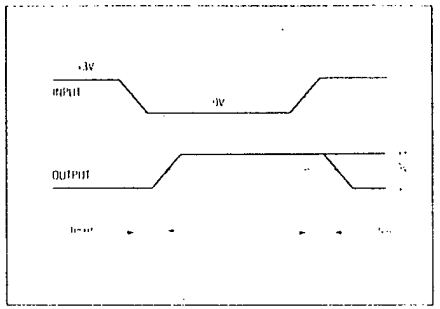


Figure 1. Transmitter Propagation Delay Timing

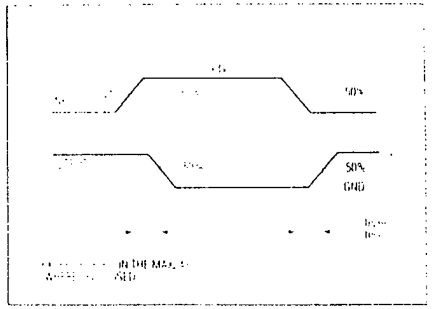


Figure 2. Receiver Propagation Delay Timing

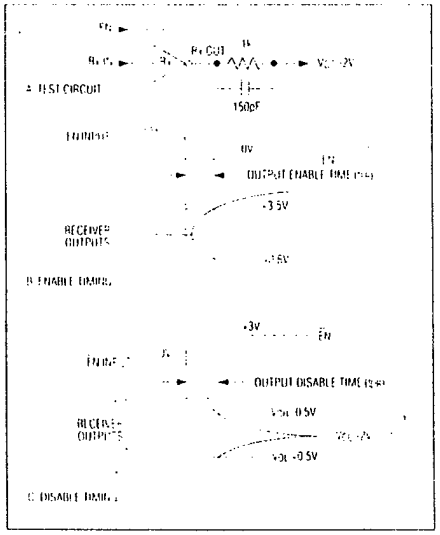


Figure 3. Receiver Output Enable and Disable Timing

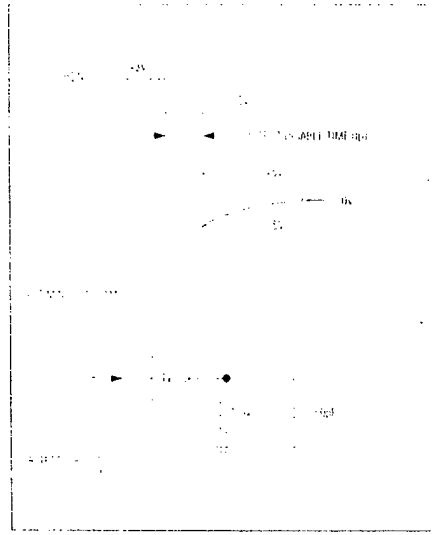


Table 1a. MAX225 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS	RECEIVERS
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All 3-State
1	0	Shutdown	All 3-State	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State

Table 1b. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1-RA4 3-State RA5 Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low Power Receiver Mode	All Low Power Receiver Mode
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receiver Mode	RB1-RB4 3-State RA5 Low-Power Receiver Mode

Table 1c. MAX246 Control Pin Configurations

$\overline{ENA}$	$\overline{ENB}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receiver Mode	RB1-RB4 3-State RA5 Low-Power Receiver Mode

Table 1d. MAX247/248/249 Control Pin Configurations

$\overline{ENTA}$	$\overline{ENTB}$	$\overline{ENRA}$	$\overline{ENRB}$	OPERATION STATUS		TRANSMITTERS		RECEIVERS	
					MAX247	TA1–TA4	TB1–TB4	RA1–RA4	RB1–RB5
					MAX248	TA1–TA4	TB1–TB4	RA1–RA4	RB1–RB4
					MAX249	TA1–TA3	TB1–TB3	RA1–RA5	RB1–RB5
0	0	0	0	Normal Operation		All Active	All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All Active	All 3-State, except RB5 stays active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State	All Active
0	0	1	1	Normal Operation		All Active	All Active	All 3-State	All 3-State, except RB5 stays active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All Active	All 3-State except RB5 stays active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State	All Active
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State	All 3-State except RB5 stays active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All Active	All 3-State, except RB5 stays active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State	All Active
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State	All 3-State except RB5 stays active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	All 3-State except RB5 stays active on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State	All 3-State, except RB5 stays active on MAX247

Detailed Description

The MAX220-MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX220-MAX249 have two internal charge-pumps that convert +5V to ±10V (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see *Typical Operating Characteristics*), except on the MAX225 and MAX245-MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA/TIA-232E driver output voltage when sourcing current from V+ and V- to external circuitry.

When using the shutdown feature in the MAX222, MAX225, MAX230, MAX235, MAX236, MAX240, MAX241 and MAX245-MAX249 avoid using V+ and V- to power external circuitry. When these parts are shut down, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ is internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA/TIA-232E and V.28 specification, that calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built-in. The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode.

The MAX239 has a receiver 3-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low-power shutdown control. The receiver TTL/CMOS outputs are in a high-impedance 3-state mode whenever the 3-state $\overline{EN}$able line is high, and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less then 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/µs unloaded and 10V/µs loaded with 3Ω and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA/TIA-232E.

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

The low-power receive-mode feature of the MAX223, MAX242, and MAX245-MAX249 puts the IC into shutdown mode, but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates. This operation conserves system power.

MAX243—Negative Threshold

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA/TIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Shutdown—MAX222-MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$) that allows receiver output control independent of $\overline{SHDN}$. With all other devices, $\overline{SHDN}$ also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. These devices have separate receiver and transmitter enable controls. The charge pumps turn off and the devices shutdown when a logic high is applied to the $\overline{ENT}$ input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the $\overline{ENR}$ input. On the MAX245, eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1-RA4 and RB1-RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

Receiver and Transmitter-Enable Control Inputs

The MAX225 and MAX245-MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

Tables 1A-1D define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

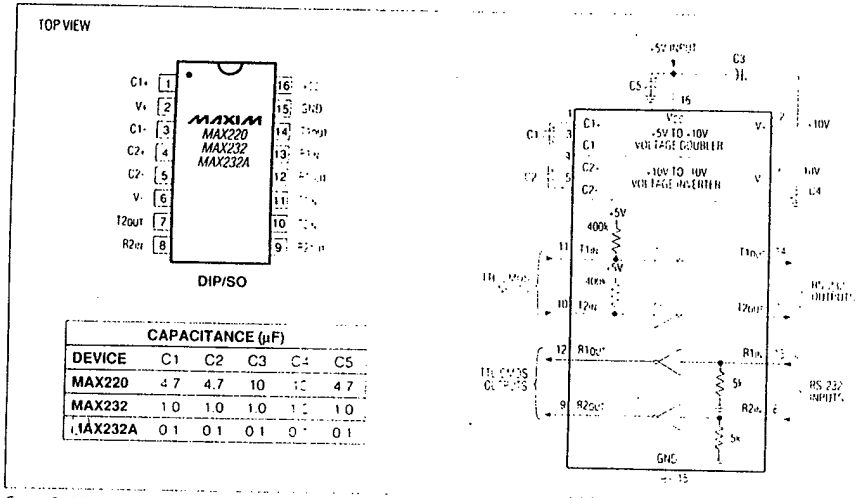
The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/s.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.



CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	[illegible]	4.7
MAX232	1.0	1.0	1.0	[illegible]	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

Figure 5 MAX220/232/232A Pin Configuration and Typical Operating Circuit

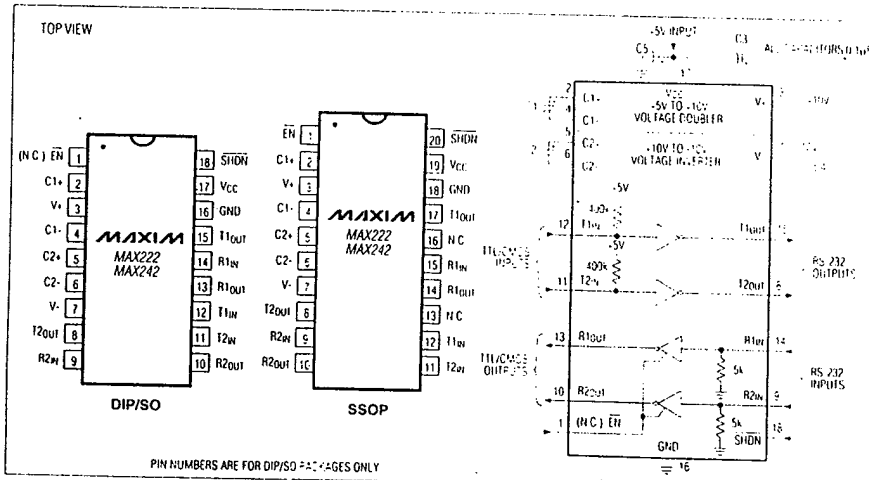
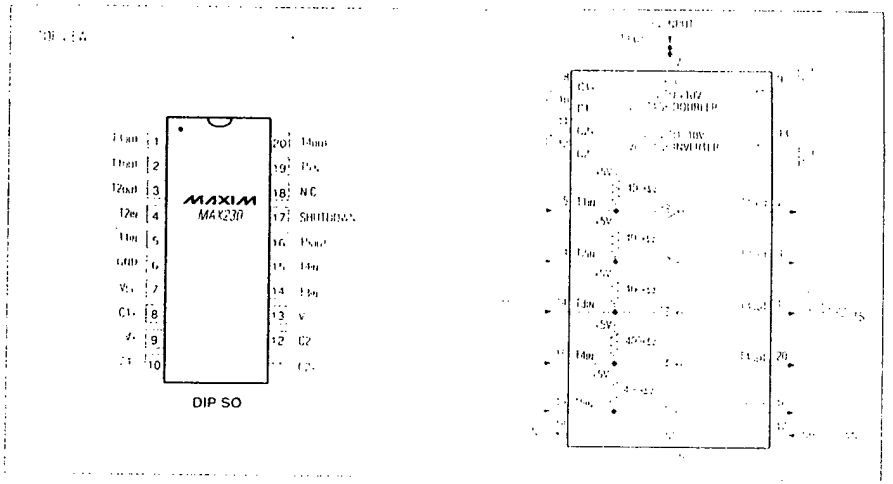
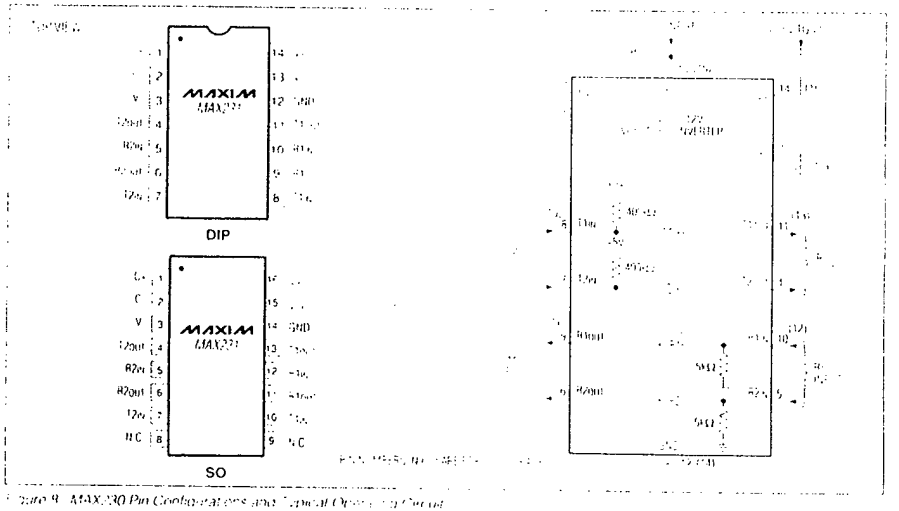


Figure 6 MAX222/MAX242 Pin Configuration and Typical Operating Circuit





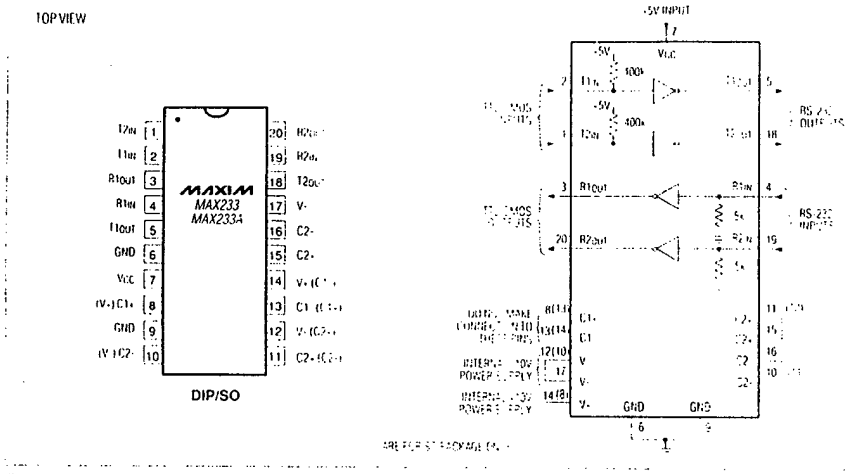


Figure 9. MAX233/MAX233A Pin Configuration and Typical Operating Circuit

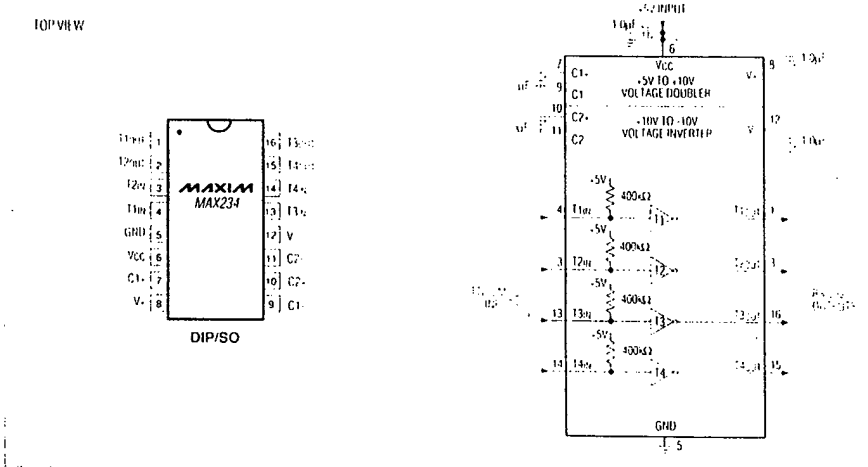
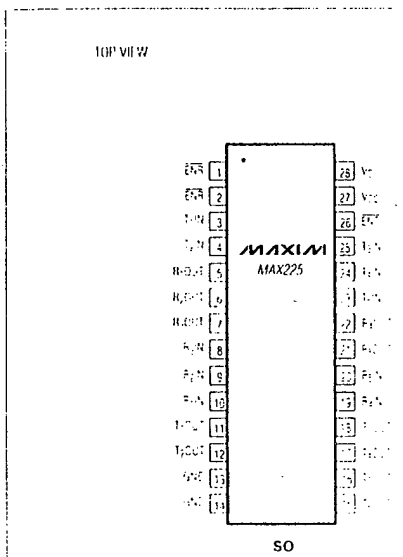


Figure 10. MAX234 Pin Configuration and Typical Operating Circuit



MAX225 Functional Description

5 Receivers

5 Transmitters

2 Control Pins

1 Receiver Enable ($\overline{ENR}$)

1 Transmitter Enable ($\overline{ENT}$)

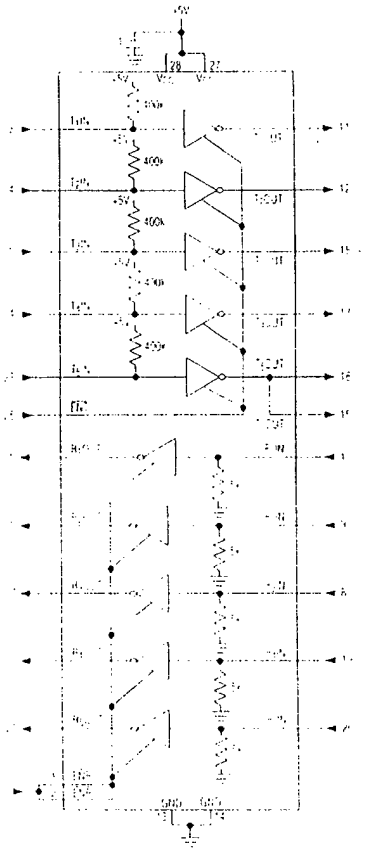


Figure 11. MAX225 Pin Configuration and Typical Operating Circuit

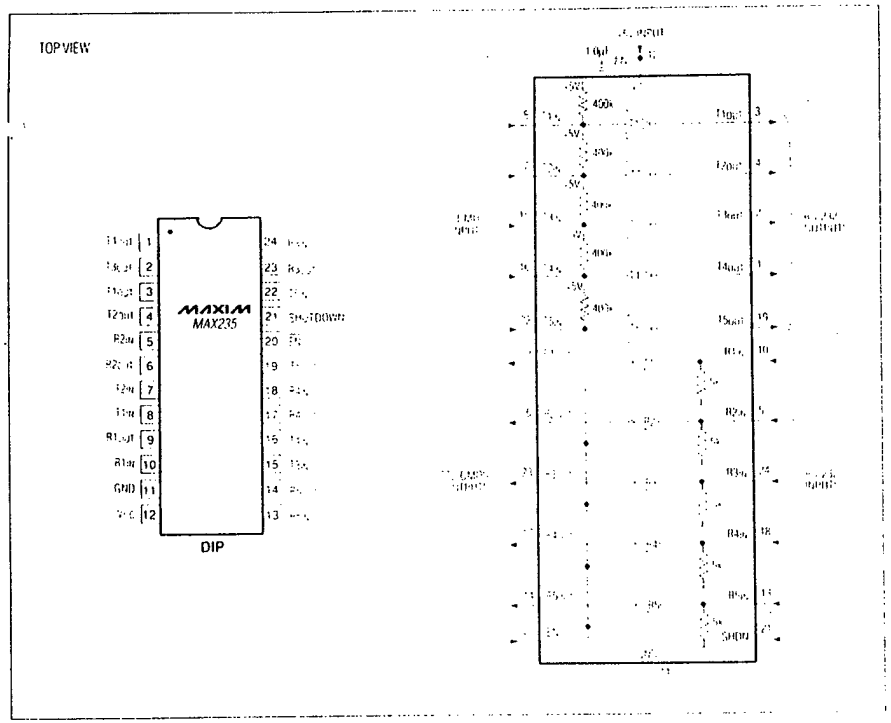


Figure 12. MAX235 Pin Configuration and Typical Operating Circuit

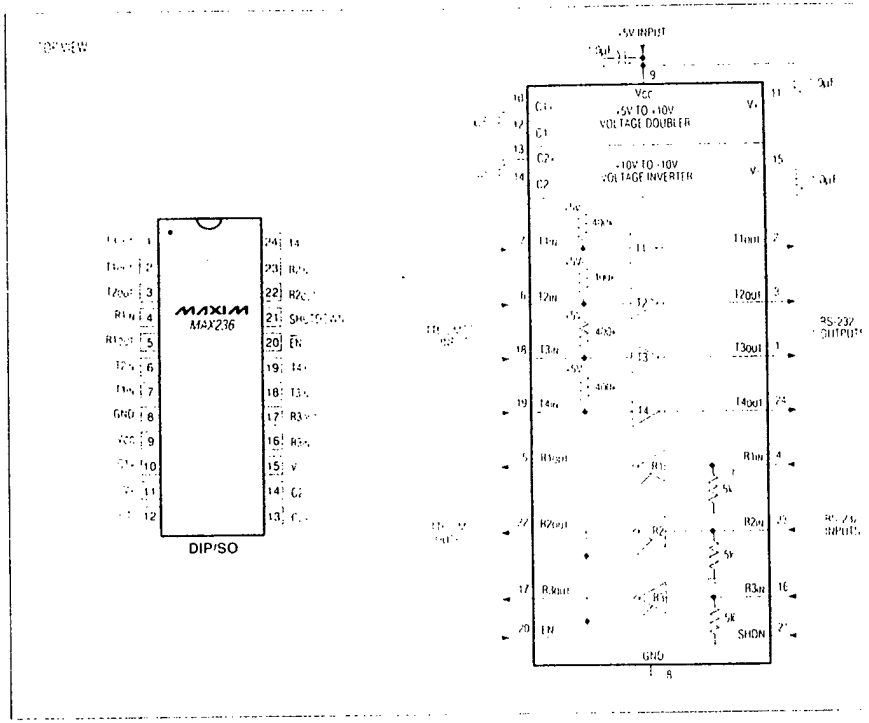


Figure 13. MAX236 Pin Configuration and Typical Operating Circuit

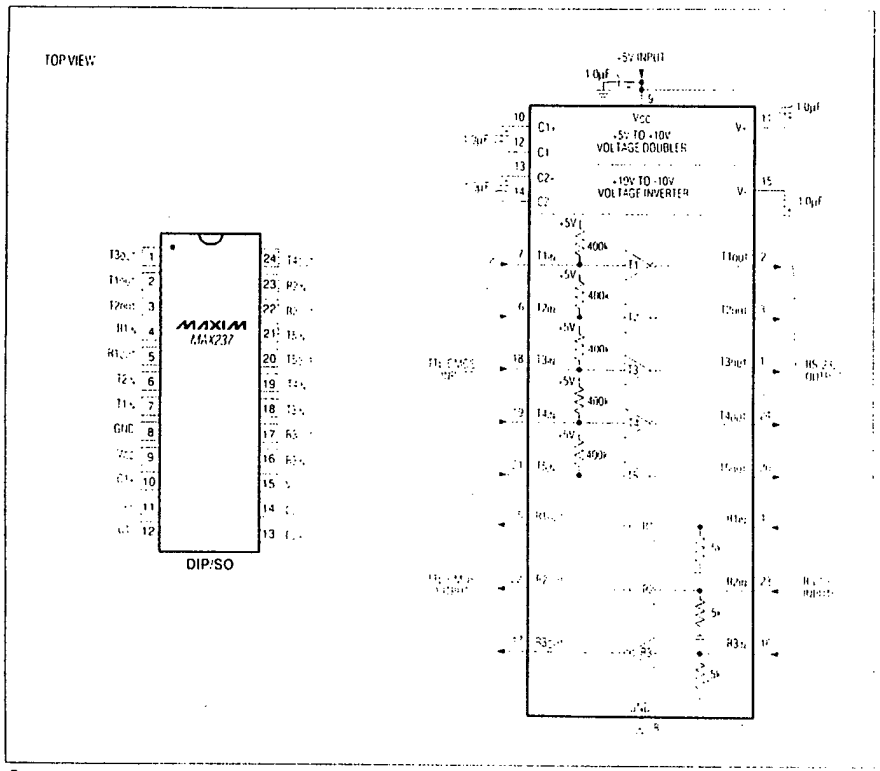


Figure 14. MAX237 Pin Configuration and Typical Operating Circuit

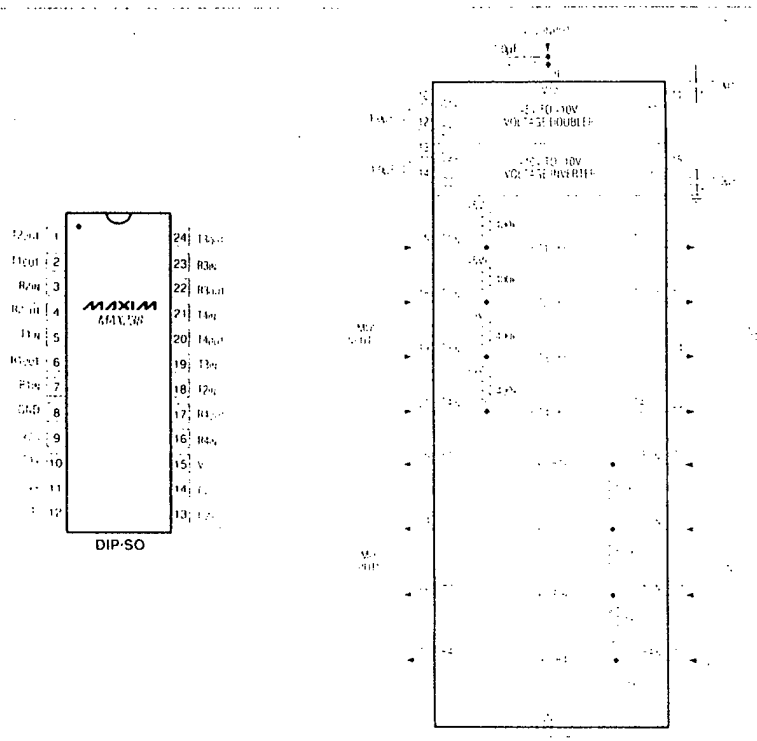


Figure 15. MAX238 Pin Configuration and Typical Operating Circuit

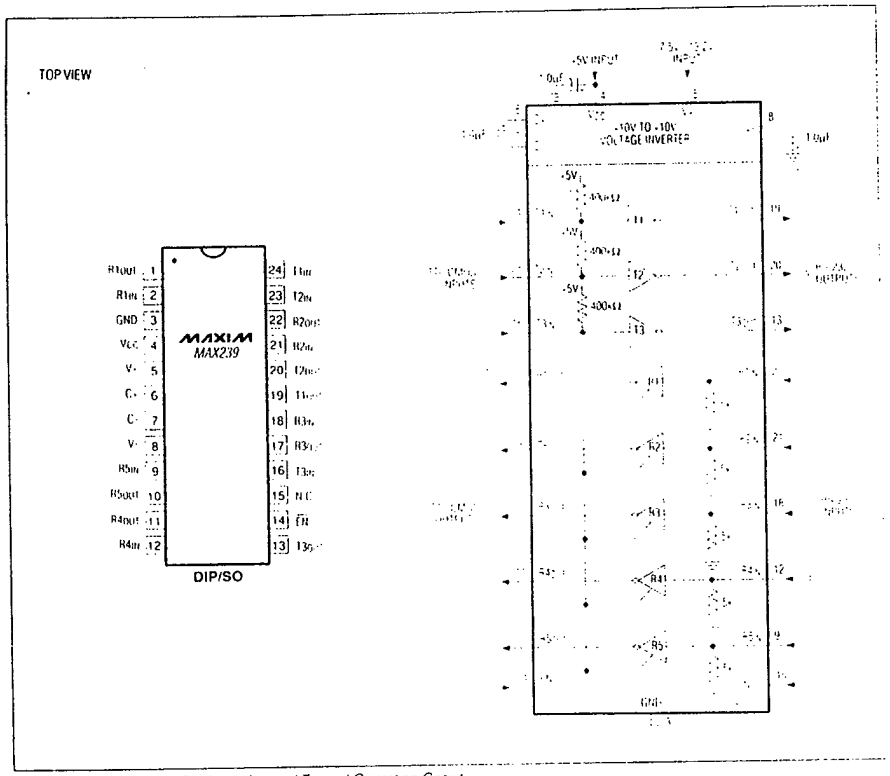


Figure 16. MAX239 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

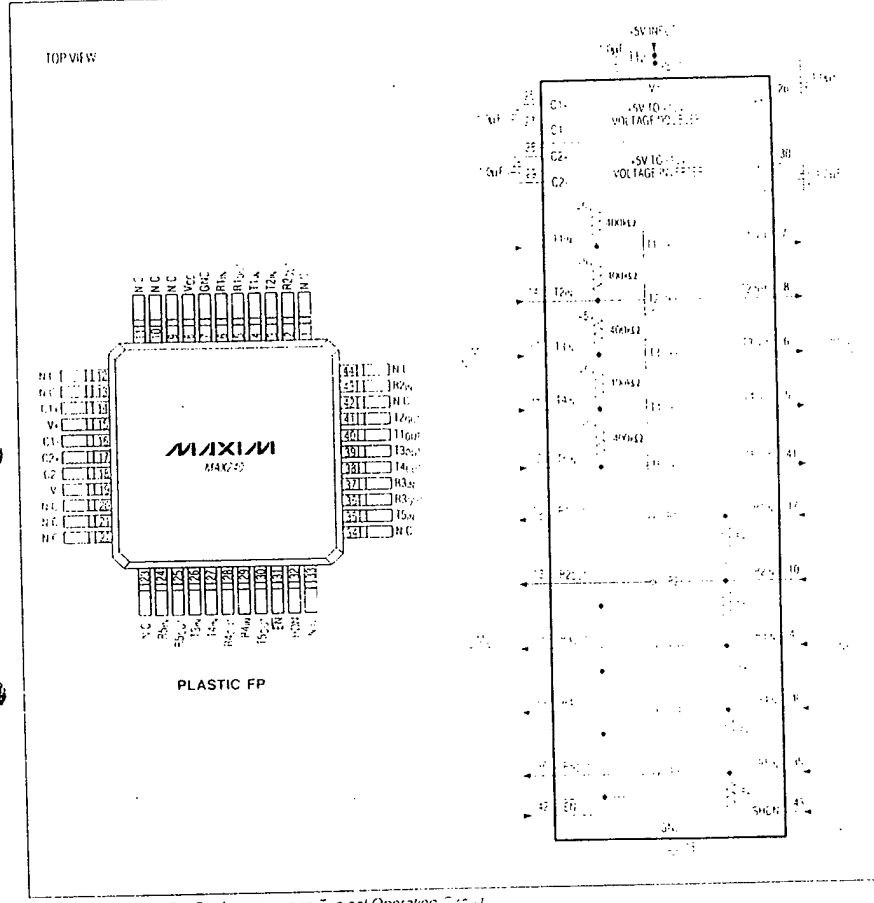


Figure 17. MAX240 Pin Configuration and Typical Operating Circuit

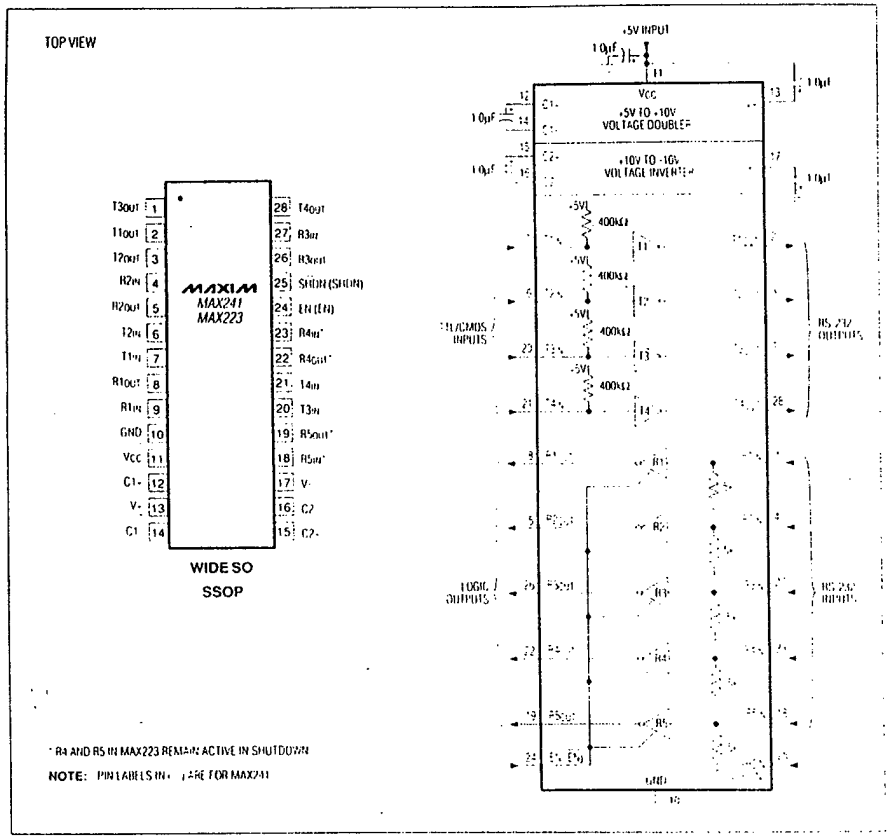


Figure 18 MAX241, MAX223 Pin Configuration and Typical Operating Circuit

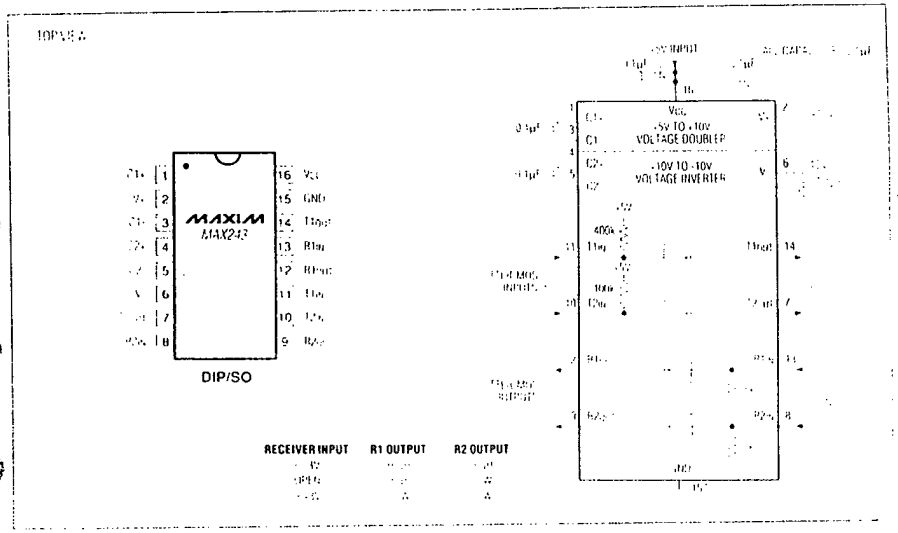
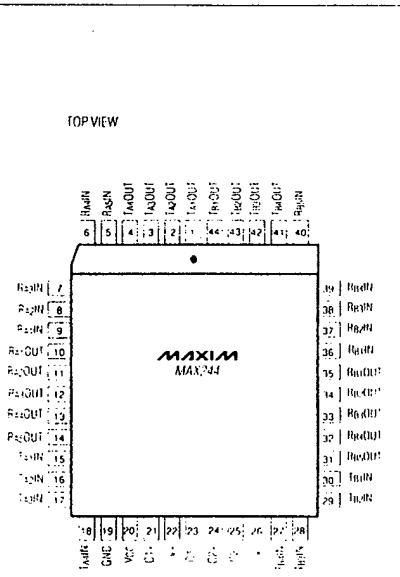
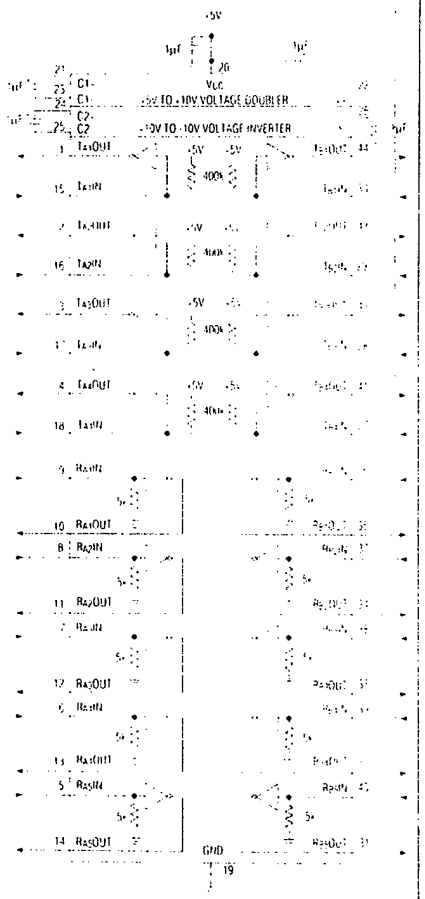


Figure 19 MAX243 Pin Configuration and Typical Operating Circuit

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers





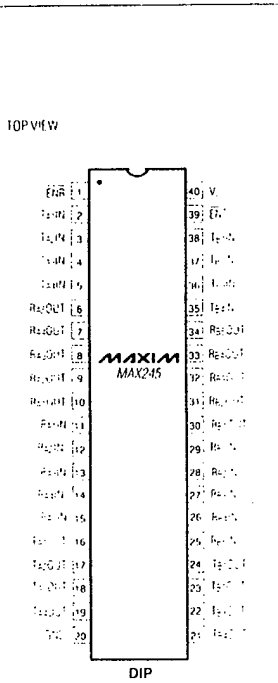
MAX244 Functional Description

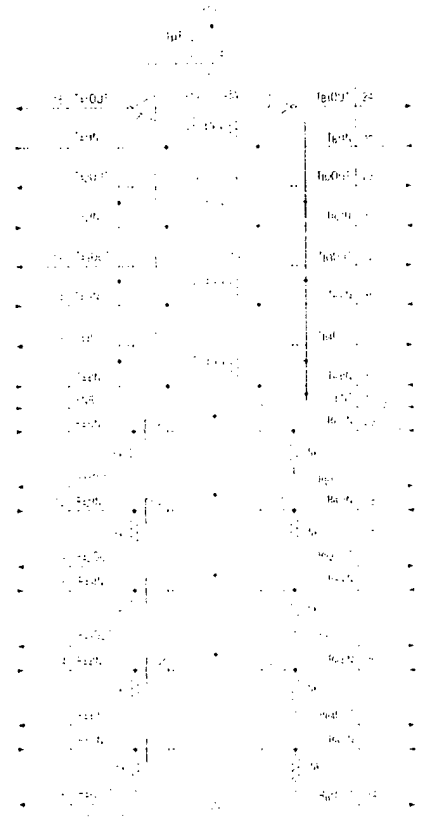
10 Receivers Always Active
- 5 A-Side Receivers
- 5 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

No Control Pins

Figure 20. MAX244 Pin Configuration and Typical Operating Circuit





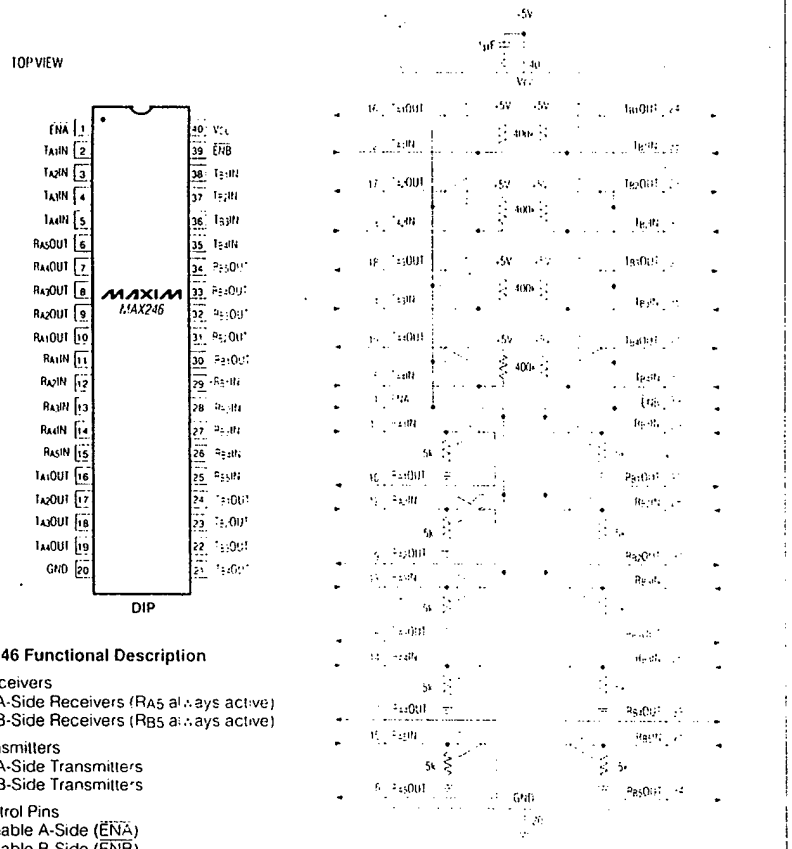
MAX245 Functional Description

10 Receivers
- 5 A-Side Receivers (RA5 always active)
- 5 B-Side Receivers (RB5 always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

2 Control Pins
- 1 Receiver Enable ($\overline{ENR}$)
- 1 Transmitter Enable ($\overline{ENT}$)

Figure 21. MAX245 Pin Configuration and Typical Operating Circuit



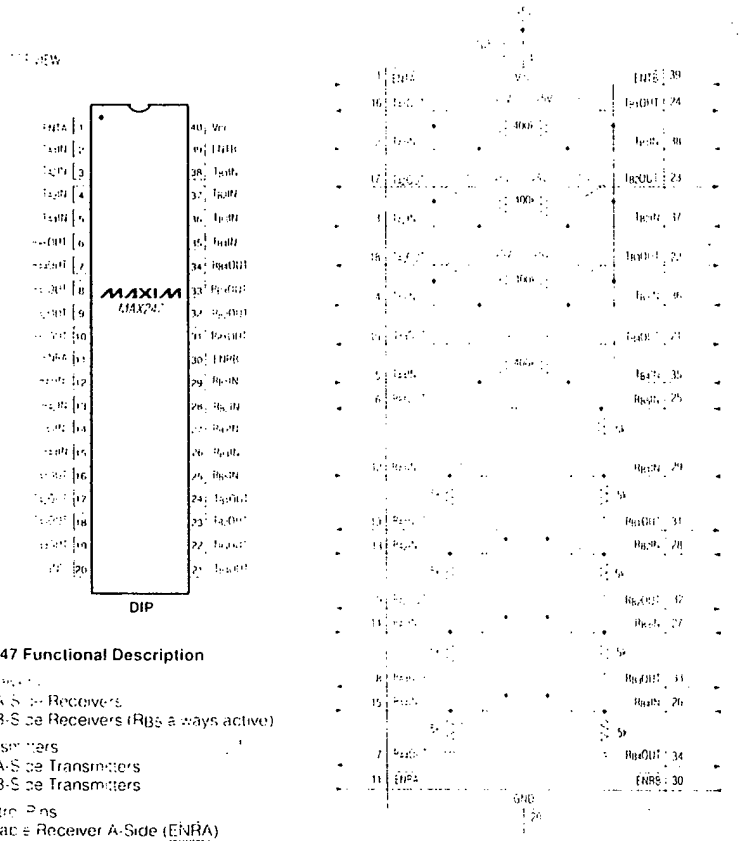
MAX246 Functional Description

10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

2 Control Pins
- Enable A-Side ($\overline{ENA}$)
- Enable B-Side ($\overline{ENB}$)

Figure 22. MAX246 Pin Configuration and Typical Operating Circuit



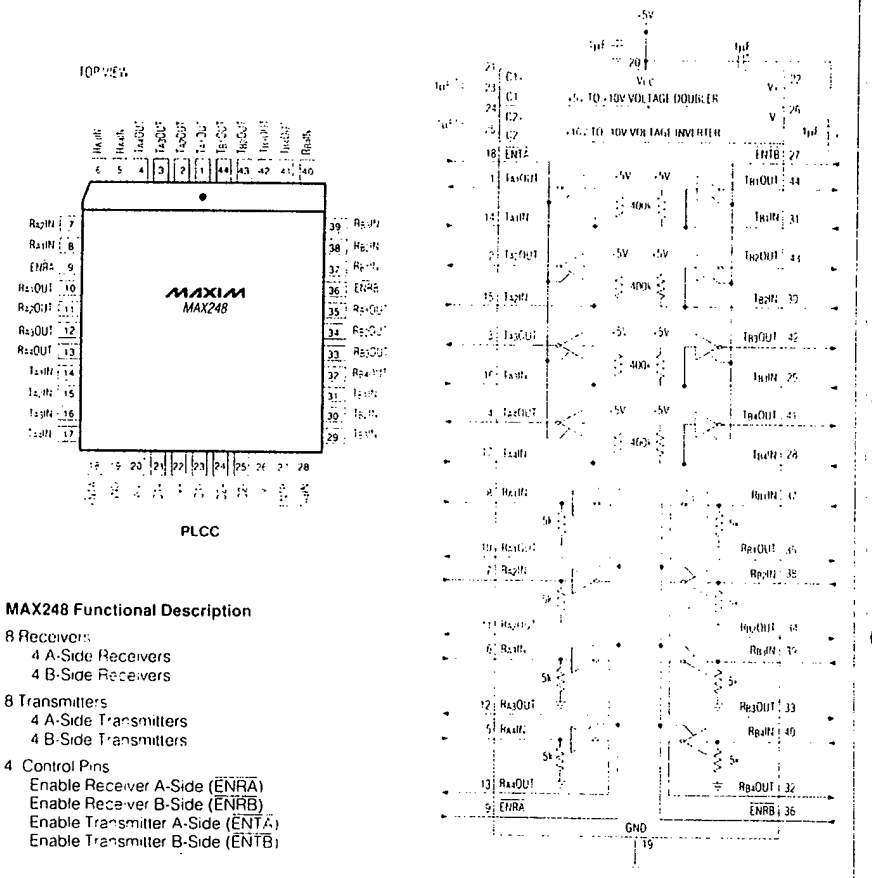
MAX247 Functional Description

- 5 A-Side Receivers
- 5 B-Side Receivers (R_{B5} always active)

- 4 A-Side Transmitters
- 4 B-Side Transmitters

- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 23. MAX247 Pin Configuration and Typical Operating Circuit



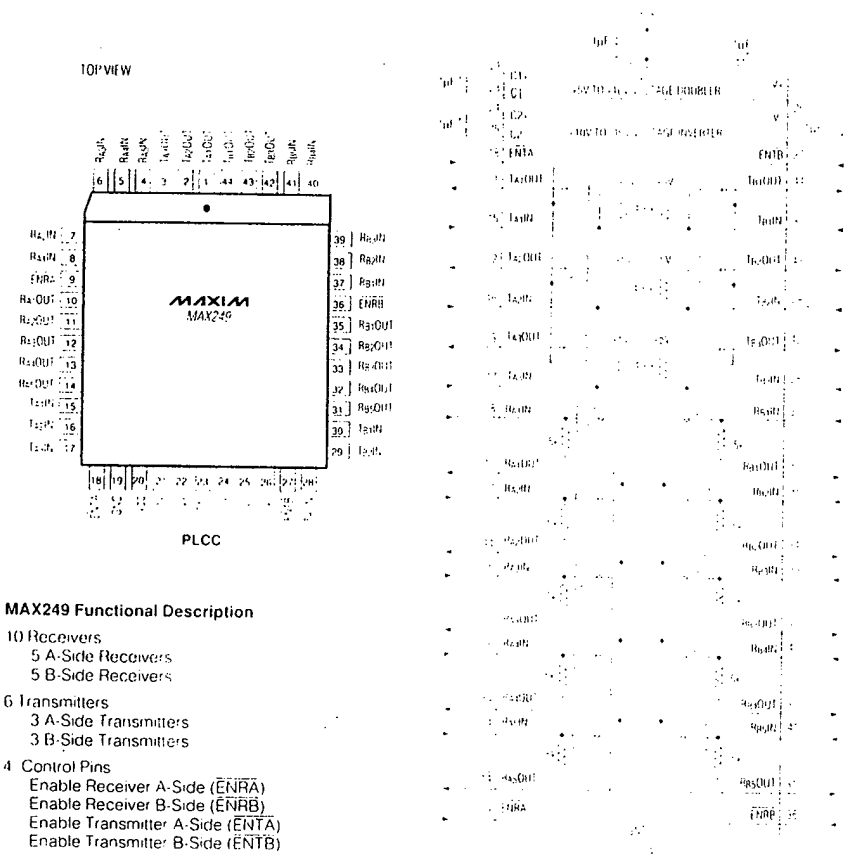
MAX248 Functional Description

8 Receivers
- 4 A-Side Receivers
- 4 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 24 MAX248 Pin Configuration and Typical Operating Circuit



MAX249 Functional Description

10 Receivers
- 5 A-Side Receivers
- 5 B-Side Receivers

6 Transmitters
- 3 A-Side Transmitters
- 3 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 25 MAX249 Pin Configuration and Typical Operating Circuit

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX222CPN	0°C to +70°C	18 Plastic DIP
MAX222CWN	0°C to +70°C	18 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	18 Plastic DIP
MAX222EWN	-40°C to +85°C	18 Wide SO
MAX222EJN	-40°C to +85°C	18 CERDIP
MAX222MJN	-55°C to +125°C	18 CERDIP
MAX223CAI	0°C to +70°C	28 SSOP
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223C/D	0°C to +70°C	Dice*
MAX223EAI	-40°C to +85°C	28 SSOP
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX225CWI	0°C to +70°C	28 Wide SO
MAX225EWI	-40°C to +85°C	28 Wide SO
MAX230CPP	0°C to +70°C	20 Plastic DIP
MAX230CWP	0°C to +70°C	20 Wide SO
MAX230C/D	0°C to +70°C	Dice*
MAX230EPP	-40°C to +85°C	20 Plastic DIP
MAX230EWP	-40°C to +85°C	20 Wide SO
MAX230EJP	-40°C to +85°C	20 CERDIP
MAX230MJP	-55°C to +125°C	20 CERDIP
MAX231CPD	0°C to +70°C	14 Plastic DIP
MAX231CWE	0°C to +70°C	16 Wide SO
MAX231CJD	0°C to +70°C	14 CERDIP
MAX231C/D	0°C to +70°C	Dice*
MAX231EPD	-40°C to +85°C	14 Plastic DIP
MAX231EWE	-40°C to +85°C	16 Wide SO
MAX231EJD	-40°C to +85°C	14 CERDIP
MAX231MJD	-55°C to +125°C	14 CERDIP
MAX232CPE	0°C to +70°C	16 Plastic DIP
MAX232CSE	0°C to +70°C	16 Narrow SO
MAX232CWE	0°C to +70°C	16 Wide SO
MAX232C/D	0°C to +70°C	Dice*
MAX232EPE	-40°C to +85°C	16 Plastic DIP
MAX232ESE	-40°C to +85°C	16 Narrow SO
MAX232EWE	-40°C to +85°C	16 Wide SO
MAX232EJE	-40°C to +85°C	16 CERDIP
MAX232MJE	-55°C to +125°C	16 CERDIP
MAX232MLP	-55°C to +125°C	20 LCC
MAX232ACPE	0°C to +70°C	16 Plastic DIP
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic DIP
MAX232AESE	-40°C to +85°C	16 Narrow SO
MAX232AEWE	-40°C to +85°C	16 Wide SO
MAX232AEJE	-40°C to +85°C	16 CERDIP
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX232AMLP	-55°C to +125°C	20 LCC
MAX233CPP	0°C to +70°C	20 Plastic DIP
MAX233EPP	-40°C to +85°C	20 Plastic DIP
MAX233ACPP	0°C to +70°C	20 Plastic DIP
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233ALPP	-40°C to +85°C	20 Plastic DIP
MAX233AEWP	40°C to +85°C	20 Wide SO
MAX234CPE	0°C to +70°C	16 Plastic DIP
MAX234CWE	0°C to +70°C	16 Wide SO
MAX234C/D	0°C to +70°C	Dice*
MAX234EPE	-40°C to +85°C	16 Plastic DIP
MAX234EWE	40°C to +85°C	16 Wide SO
MAX234EJE	40°C to +85°C	16 CERDIP
MAX234MJE	-55°C to +125°C	16 CERDIP
MAX235CPG	0°C to +70°C	24 Wide Plastic DIP
MAX235EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX235EDG	40°C to +85°C	24 Ceramic SB
MAX235MDG	-55°C to +125°C	24 Ceramic SB
MAX236CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX236CWG	0°C to +70°C	24 Wide SO
MAX236C/D	0°C to +70°C	Dice*
MAX236ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX236EWG	-40°C to +85°C	24 Wide SO
MAX236ERG	40°C to +85°C	24 Narrow CERDIP
MAX236MRG	-55°C to +125°C	24 Narrow CERDIP
MAX237CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX237CWG	0°C to +70°C	24 Wide SO
MAX237C/D	0°C to +70°C	Dice*
MAX237ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX237EWG	-40°C to +85°C	24 Wide SO
MAX237ERG	-40°C to +85°C	24 Narrow CERDIP
MAX237MRG	-55°C to +125°C	24 Narrow CERDIP
MAX238CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX238CWG	0°C to +70°C	24 Wide SO
MAX238C/D	0°C to +70°C	Dice*
MAX238ENG	-40°C to +85°C	24 Narrow Plastic DIP

*Contact factory for dice specifications

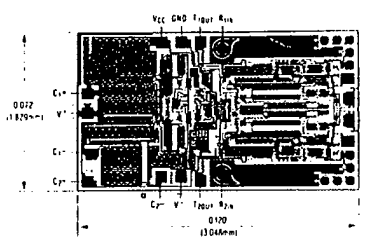
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX238EWG	-40°C to +85°C	24 Wide SO
MAX238ERG	-40°C to +85°C	24 Narrow CERDIP
MAX238MRG	-55°C to +125°C	24 Narrow CERDIP
MAX239CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX239CWG	0°C to +70°C	24 Wide SO
MAX239C/D	0°C to +70°C	Dice*
MAX239ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX239EWG	-40°C to +85°C	24 Wide SO
MAX239ERG	-40°C to +85°C	24 Narrow CERDIP
MAX239MRG	-55°C to +125°C	24 Narrow CERDIP
MAX240CMH	0°C to +70°C	44 Plastic FP
MAX240C/D	0°C to +70°C	Dice*
MAX241CAI	0°C to +70°C	28 SSOP
MAX241CWI	0°C to +70°C	28 Wide SO
MAX241C/D	0°C to +70°C	Dice*
MAX241EAI	40°C to +85°C	28 SSOP
MAX241EWI	40°C to +85°C	28 Wide SO
MAX242CAP	0°C to +70°C	20 SSOP
MAX242CPN	0°C to +70°C	18 Plastic DIP
MAX242CWN	0°C to +70°C	18 Wide SO
MAX242C/D	0°C to +70°C	Dice*
MAX242EPN	-40°C to +85°C	18 Plastic DIP
MAX242EWN	-40°C to +85°C	18 Wide SO
MAX242EJN	-40°C to +85°C	18 CERDIP
MAX242MJN	-55°C to +125°C	18 CERDIP
MAX243CPE	0°C to +70°C	16 Plastic DIP
MAX243CSE	0°C to +70°C	16 Narrow SO
MAX243CWE	0°C to +70°C	16 Wide SO
MAX243C/D	0°C to +70°C	Dice*
MAX243EPE	-40°C to +85°C	16 Plastic DIP
MAX243ESE	-40°C to +85°C	16 Narrow SO
MAX243EWE	-40°C to +85°C	16 Wide SO
MAX243EJE	-40°C to +85°C	16 CERDIP
MAX243MJE	-55°C to +125°C	16 CERDIP
MAX244CQH	0°C to +70°C	44 PLCC
MAX244C/D	0°C to +70°C	Dice*
MAX244EQH	-40°C to +85°C	44 PLCC
MAX245CPL	0°C to +70°C	40 Plastic DIP
MAX245C/D	0°C to +70°C	Dice*
MAX245EPL	-40°C to +85°C	40 Plastic DIP
MAX246CPL	0°C to +70°C	40 Plastic DIP
MAX246C/D	0°C to +70°C	Dice*
MAX246EPL	-40°C to +85°C	40 Plastic DIP
MAX247CPL	0°C to +70°C	40 Plastic DIP
MAX247C/D	0°C to +70°C	Dice*
MAX247EPL	-40°C to +85°C	40 Plastic DIP
MAX248CQH	0°C to +70°C	44 PLCC
MAX248C/D	0°C to +70°C	Dice*
MAX248EQH	-40°C to +85°C	44 PLCC
MAX249CQH	0°C to +70°C	44 PLCC
MAX249EQH	-40°C to +85°C	44 PLCC

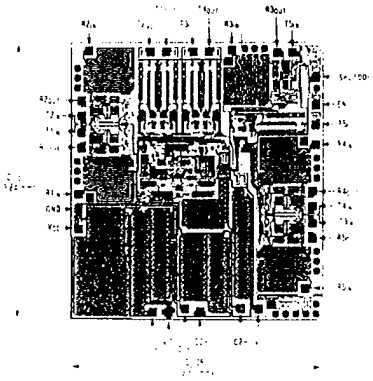
*Contact factory for dice specifications

+5V-Powered, Multi-Channel RS-232 Drivers/Receivers

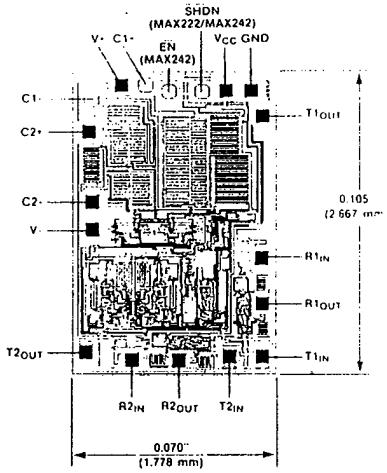
Chip Topographies



MAX231, MAX232 and MAX233

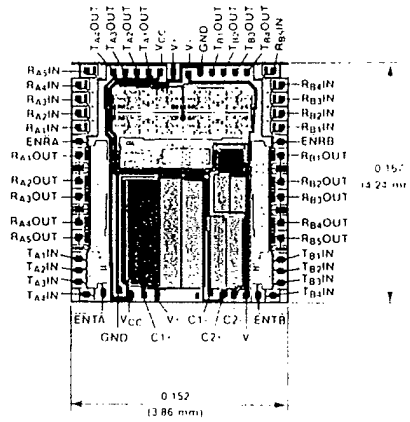


MAX230 and MAX234-239, MAX240, MAX241



MAX220/222/232A/233A/242/243

CONNECT SUBSTRATE TO V+



MAX244/245 246/247/248/249

HARRIS SEMICONDUCTOR

HS-82C55ARH

Radiation Hardened CMOS Programmable Peripheral Interface

September 1995

Features

- Radiation Hardened
  - Total Dose >10^5 RAD (Si)
  - Transient Upset <10^8 RAD (Si)/s
  - Latch Up Free EPI-CMOS
- Low Power Consumption
  - IDDSB = 20µA
- Pin Compatible with NMOS 8255A and the Harris 82C55A
- High Speed, No "Wait State" Operation with 5MHz HS-80C86RH
- 24 Programmable I/O Pins
- Bus-Hold Circuitry on All I/O Ports Eliminates Pull-Up Resistors
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- 2.0mA Drive Capability on All I/O Port Outputs
- Military Temperature Range: -55°C to +125°C

Description

The Harris HS-82C55ARH is a high performance, radiation hardened CMOS version of the industry standard 8255A and is manufactured using a hardened field, self-aligned silicongate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which are organized into two 8-bit and two 4-bit ports. Each port may be programmed to function as either an input or an output. Additionally, one of the 8-bit ports may be programmed for bi-directional operation,and the two 4-bit ports can be programmed to provide handshaking capabilities. The high performance, radiation hardness, and industry standard configuration of the HS-82C55ARH make it compatible with the HS-80C86RH radiation hardened microprocessor.

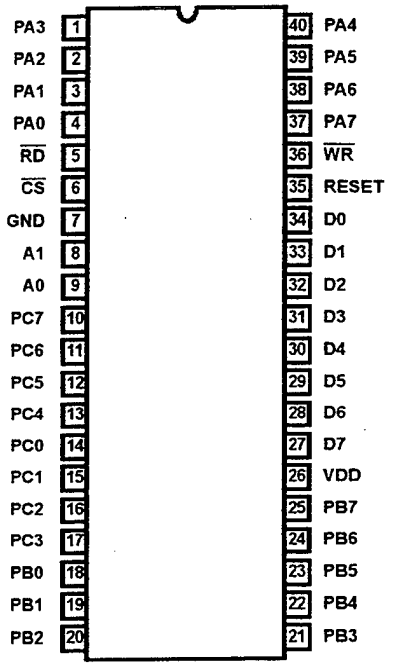
Static CMOS circuit design insures low operating power. Bus hold circuitry eliminates the need for pull-up resistors. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
HS1-82C55ARH-Q	-55°C to +125°C	40 Lead SBDIP
HS1-82C55ARH-8	-55°C to +125°C	40 Lead SBDIP
HS1-82C55ARH/Sample	+25°C	40 Lead SBDIP

Pinout

40 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T40
TOP VIEW



Pin Description

PIN	DESCRIPTION
D7 - D0	Data Bus (Bi-Directional
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0 - A1	Port Address
PA7 - PA0	Port A (Bit)
PB& - PB0	Port B (Bit)
PC7 - PC0	Port C (Bit)
VDD	+5 volts
GND	0 volts

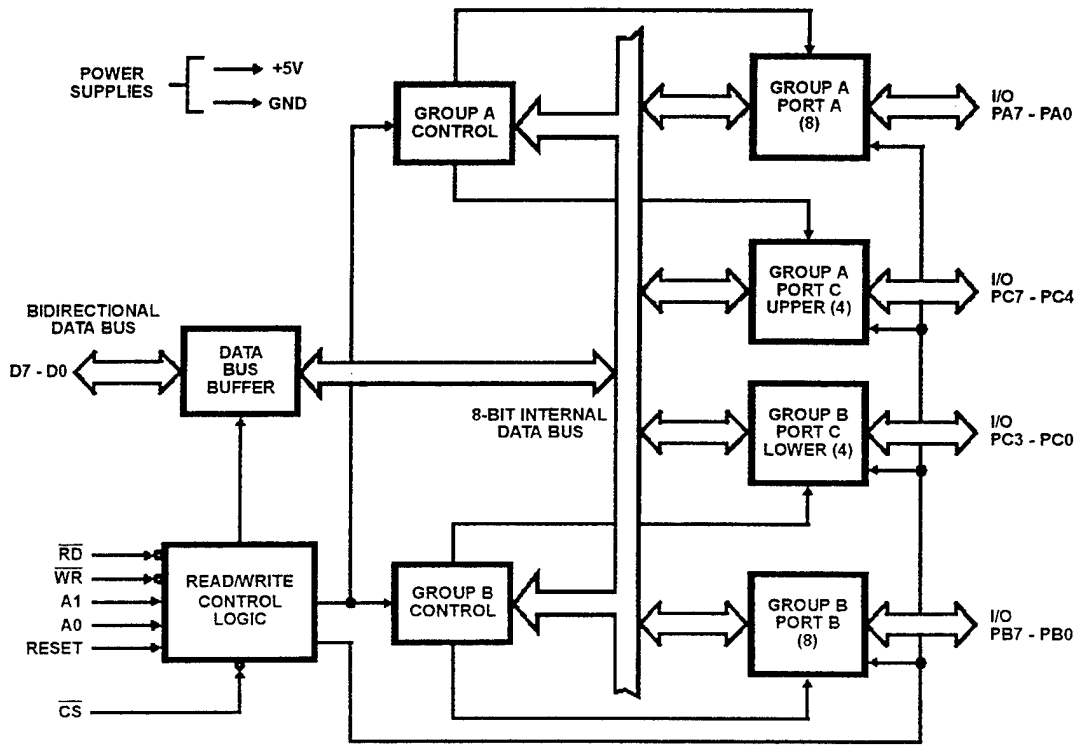
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures

Spec Number 518060
File Number 3191.1

Pin Description

SYMBOL	PIN NUMBERS	TYPE	DESCRIPTION
PA0-7	1-4, 37-40	I/O	**Port A:** General purpose I/O Port. Data direction and mode is determined by the contents of the Control Word.
PB0-7	18-25	I/O	**Port B:** General purpose I/O port. See Port A.
PC0-3	14-17	I/O	**Port C (Lower):** Combination I/O port and control port associated with Port B. See Port A.
PC4-7	10-13	I/O	**Port C (Upper):** Combination I/O Port and control port associated with Port A. See Port A.
D0-7	27-34	I/O	**Bidirectional Data Bus:** Three-State data bus enabled as an input when $\overline{CS}$ and $\overline{WR}$ are low and as an output when $\overline{CS}$ and $\overline{RD}$ are low.
VDD	26	I	**VDD:** The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7	I	**Ground.**
CS	6	I	**Chip Select:** A "low" on this input pin enables the communication between the HS-82C55ARH and the CPU.
RD	5	I	**Read:** A "low" on this input pin enables the HS-82C55ARH to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the HS-82C55ARH.
WR	36	I	**Write:** A "low" on this input pin enables the CPU to write data or control words into the HS-82C55ARH.
A0 and A1	8, 9	I	**Port Select 0 and Port Select 1:** These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the Least Significant Bits of the address bus (A0 and A1).
Reset	35	I	**Reset:** A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the HS-82C55ARH will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400µA.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . VSS-0.3V to VDD+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C
ESD Classification . . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	40°C/W	6°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 1.25W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package 25.0mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . VDD -1.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
TTL Output High Voltage	VOH1	VDD = 4.5V, IO = -2.5mA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	3.0	-	V
CMOS Output High Voltage	VOH2	VDD = 4.5V, IO = -100µA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD-0.4	-	V
Output Low Voltage	VOL	VDD = 4.5V, IO = 2.5mA, VIN = 0V, 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-10	10	µA
Input Current Bus Hold High	IBHH	VDD = 4.5V or 5.5V, VIN = 3.0V (See Note 1) Ports A, B, C	1, 2, 3	-55°C, +25°C, +125°C	-800	-60	µA
Input Current Bus Hold Low	IBHL	VDD = 4.5V or 5.5V, VIN = 1.0V (See Note 2) Port A	1, 2, 3	-55°C, +25°C, +125°C	60	800	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VIN =GND or VDD	1, 2, 3	-55°C, +25°C, +125°C	-	20	µA
Darlington Drive Voltage	VDAR	VDD = 4.5V, IO = -2.0mA, VIN = GND or VDD	1, 2, 3	-55°C, +25°C, +125°C	3.9	-	V
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test (Note 4)	FN	VDD = 5.5V, VIN = GND or VDD - 1.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTES:

1. IBHH should be measured after raising VIN and then lowering to 3.0V.
2. IBHL should be measured after lowering VIN to VSS and then raising to 0.8V.
3. No internal current limiting exists on the Port Outputs. A resistor must be added externally to limit the current.
4. For VIH (VDD = 5.5V) and VIL (VDD = 4.5V) each of the following groups is tested separately with all other inputs using VIH = 2.6V, VIL = 0.4V: PA, PB, PC, Control Pins (Pins 5, 6, 8, 9, 35, 36).

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS T_A = -55°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
READ							
Address Stable Before $\overline{RD}$	TAVRL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Stable After $\overline{RD}$	TRHAX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{RD}$ Pulse Width	TRLRH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	250	-	ns
Data Valid From $\overline{RD}$	TRLDV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
Data Float After $\overline{RD}$	TRHDX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns
Time Between $\overline{RD}$s and/ or $\overline{WR}$s	TRWHRWL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	300	-	ns
WRITE							
Address Stable Before $\overline{WR}$	TAVWL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Address Stable After $\overline{WR}$	TWHAX	VDD = 4.5, 5.5V, Ports A and B	9, 10, 11	-55°C, +25°C, +125°C	20	-	ns
		VDD = 4.5, 5.5V, Port C	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
$\overline{WR}$ Pulse Width	TWLWH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Data Valid to $\overline{WR}$ High	TDVWH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Data Valid After $\overline{WR}$ High	TWHDX	VDD = 4.5, 5.5V, Ports A and B	9, 10, 11	-55°C, +25°C, +125°C	30	-	ns
		VDD = 4.5, 5.5V, Port C	9, 10, 11	-55°C, +25°C, +125°C	100	-	
OTHER TIMINGS							
$\overline{WR}$ = 1 to Output	TWHPV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	350	ns
Peripheral Data Before $\overline{RD}$	TPVRL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
Peripheral Data After $\overline{RD}$	TRHPX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{ACK}$ Pulse Width	TKLKH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
$\overline{STB}$ Pulse Width	TSLSH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	100	-	ns
Peripheral Data Before $\overline{STB}$ High	TPVSH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	20	-	ns
Peripheral Data After $\overline{STB}$ High	TSHPX	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	50	-	ns
$\overline{ACK}$ = 0 to Output	TKLPV	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	175	ns
$\overline{ACK}$ = 1 to output Float	TKHPZ	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	10	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS T_A = -55°C to +125°C (Continued)

PARAMETER	SYMBOL	CONDITIONS	SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
$\overline{WR}$ = 1 to $\overline{OBF}$ = 0	TWHOL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1	TKLOH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{STB}$ = 0 to IBF = 1	TSLIH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{RD}$ = 1 to IBF = 0	TRHIL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{RD}$ = 0 to INTR = 1	TRLNL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
$\overline{STB}$ = 1 t INTR = 1	TSHNH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{ACK}$ = 1 to INTR = 1	TKHNH	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	150	ns
$\overline{WR}$ = 0 to INTR = 0	TWLNL	VDD = 4.5, 5.5V	9, 10, 11	-55°C, +25°C, +125°C	-	200	ns
RESET Pulse Width	TRSHRSL	VDD = 4.5, 5.5V (Note 2)	9, 10, 11	-55°C, +25°C, +125°C	500	-	ns

NOTES:

1. AC's tested at worst case VDD, guaranteed over full operating range.
2. Period of initial RESET pulse after power-on must be at least 50µs. Subsequenct RESET pulses may be 500ns minimum.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz, All measurements referenced to device ground	T_A = +25°C	-	10	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz, All measurements referenced to device ground	T_A = +25°C	-	20	pF
Data Float After $\overline{RD}$	TRHDX	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	75	ns
$\overline{ACK}$ = 1 to Output Float	TKHPZ	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	-	250	ns

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics

TALBE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

See +25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7, 9)

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	±10µA
Input Leakage Current	IIL, IIH	±200nA
Output Leakage Current	IOZL, IOZH	±2µA
Low Level Output Voltage	VOL	±80mV
TTL Output High Voltage	VOH1	±600mV
CMOS Output High Voltage	VOH2	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9	-	N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

CSI and/or GSI PreCap (Note 6)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 1)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 2)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 4)

Sample - Group D, Method 5005 (Notes 4 and 5)

100% Data Package Generation (Note 7)

CSI and/or GSI Final (Note 6)

NOTES:

1. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
2. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
4. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group B Samples, Group D Test and Group D Samples.
5. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
6. CSI and/or GSI inspections are optional and will not be performed unless required by theP.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
7. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

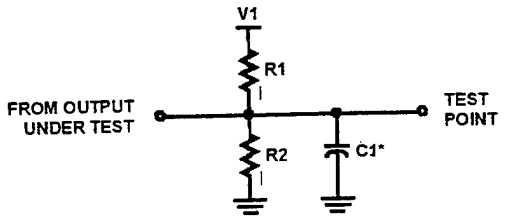
Harris Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects
100% Die Attach
Periodic- Wire Bond Pull Monitor, Method 2011
Periodic- Die Shear Monitor, Method 2019 or 2027
100% Internal Visual Inspection, Method 2010, Condition B
CSI an/or GSI PreCap (Note 5)
100% Temperature Cycle, Method 1010, Condition C, 10 Cycles
100% Constant Acceleration, Method 2001, Condition per Method 5004
100% External Visual
100% Initial Electrical Test
100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015
100% Interim Electrical Test
100% PDA, Method 5004 (Note 1)
100% Final Electrical Test
100% Fine/Gross Leak, Method 1014
100% External Visual, Method 2009
Sample - Group A, Method 5005 (Note 2)
Sample - Group B, Method 5005 (Note 3)
Sample - Group C, Method 5005 (Notes 3 and 4)
Sample - Group D, Method 5005 (Notes 3 and 4)
100% Data Package Generation (Note 6)
CSI and/or GSI Final (Note 5)

NOTES:

1. Failures from subgroup 1, 7 are used for calculating PDA. The maximum allowable PDA = 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
3. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
4. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
5. CSI and/or GSI inspections are optional and will not be performed unless required by theP.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
6. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Group B, C and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Test Circuit

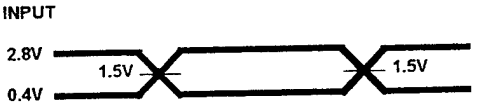


* Includes stray and jig capacitance

TEST CONDITIONS DEFINITION TABLE

V1	R1	R2	C1
1.7V	523Ω	Open	150pF

AC Testing Input, Output Waveforms



NOTE: AC Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1V/ns.

Waveforms

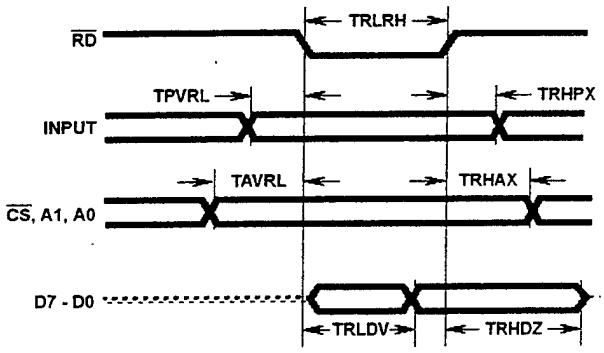


FIGURE 1. MODE 0 (BASIC INPUT)

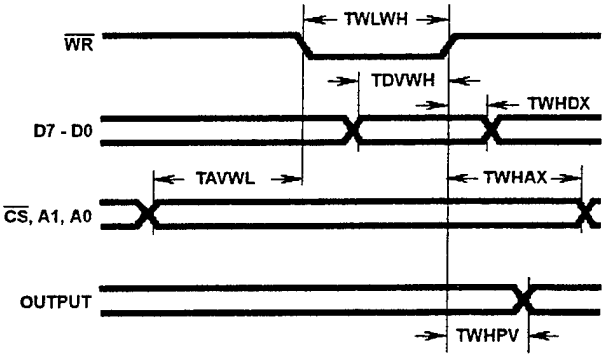


FIGURE 2. MODE 0 (BASIC OUTPUT)

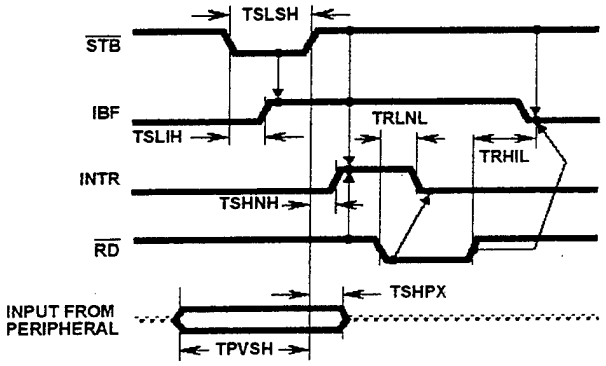


FIGURE 3. MODE 1 (STROBED INPUT)

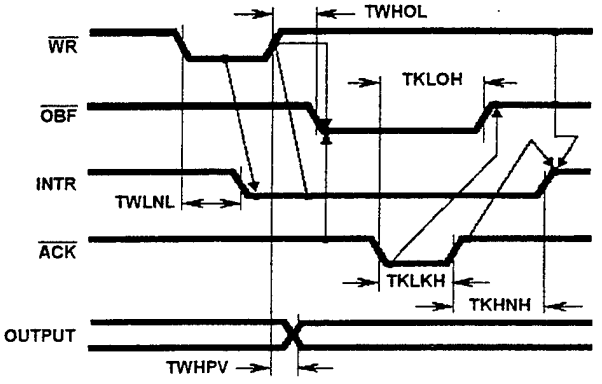


FIGURE 4. MODE 1 (STROBED OUTPUT)

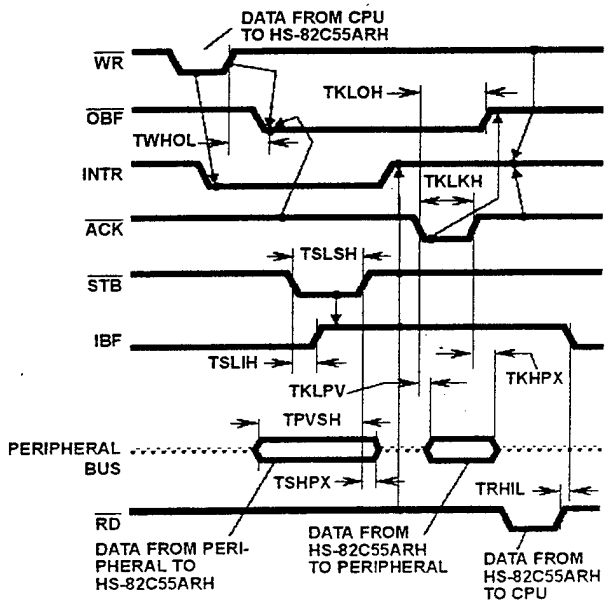


FIGURE 5. MODE 2 (BIDIRECTIONAL)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

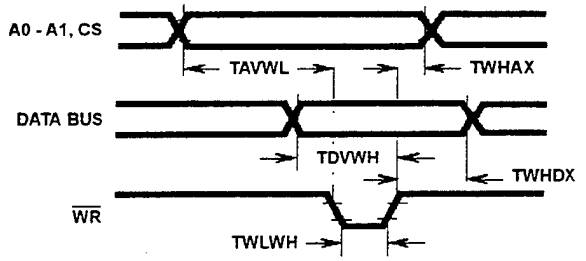


FIGURE 6. WRITE TIMING

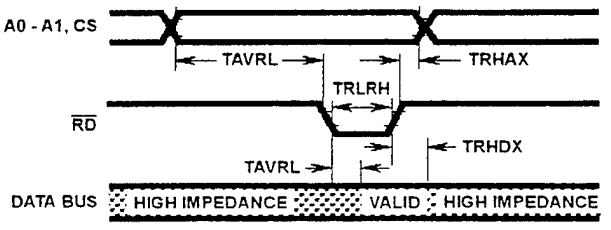
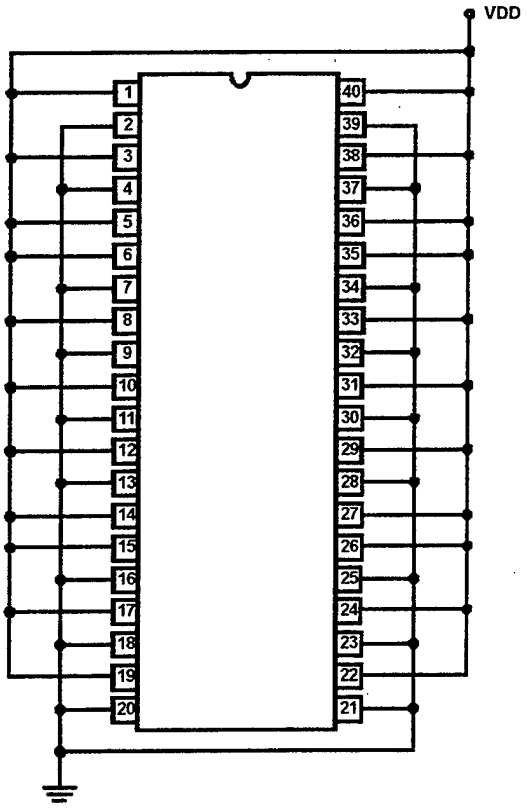


FIGURE 7. READ TIMING

Burn-In Circuits

PROGRAMMABLE PERIPHERAL INTERFACE

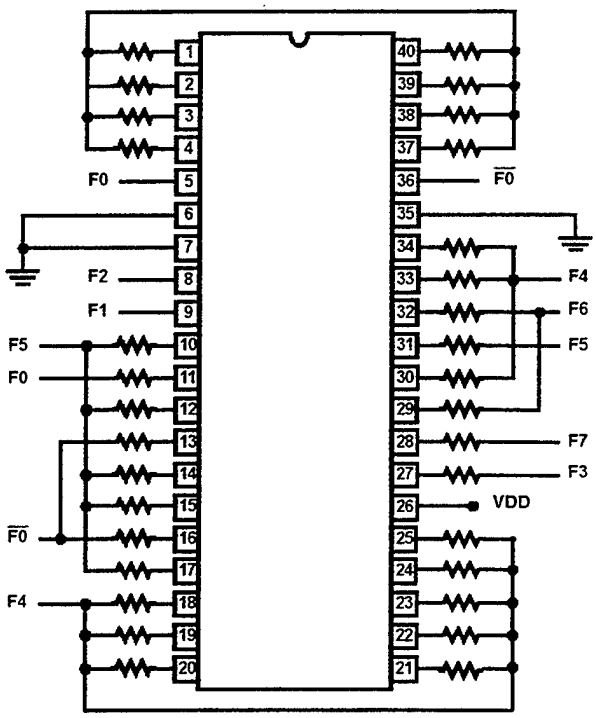


STATIC CONFIGURATION

NOTES:

1. VDD = 6.0V ± 0. 5%
2. IDD <500µA
3. T_A Min = +125°C

PROGRAMMABLE PERIPHERAL INTERFACE



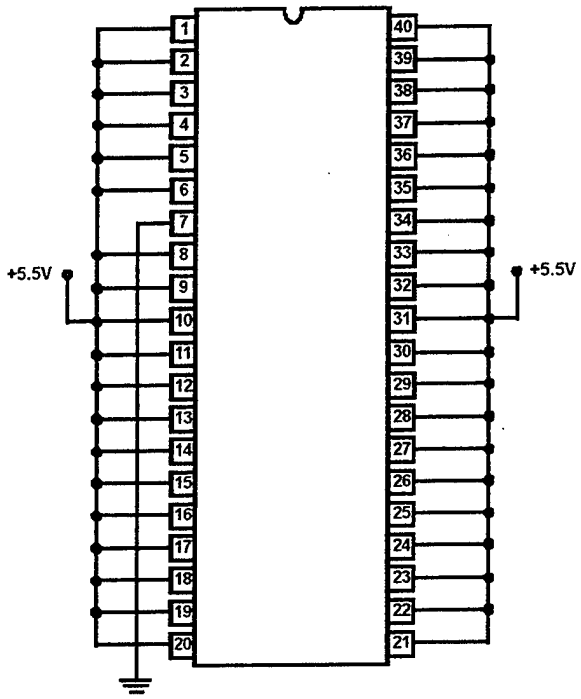
DYNAMIC CONFIGURATION

NOTES:

1. VDD = 6.0V ± 5% for Burn-In
2. VDD = 5.0V ± 5% for Life Test
3. All resistors are 10KΩ ± 5%
4. -0.3V ≤ VIL ≤ 0.8V
5. VDD - 1.0V ≤ VIH ≤ VDD
6. IDD < 5mA
7. F0 = 10KHz, 50% Duty cycle
8. F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2 . . . F7 = F6/2
9. T_A Min = +125°C

Irradiation Circuit

CMOS PROGRAMMABLE PERIPHERAL INTERFACE



NOTE:

1. VDD = 5.5V

Functional Description

The HS-82C55ARH is a programmable peripheral interface designed to allow microcomputer systems to control and interface with all types of peripheral devices.It has the ability to generate and respond to all asynchronous handshaking signals necessary to transfer data to and from peripheral devices, and it can also interrupt the processor when a peripheral needs servicing. These capabilities allow the HS-82C55ARH to be used in an unlimited number of applications including EXTERNAL SYSTEM CONTROL, ASYNCHRONOUS DATA TRANSFER, and SYSTEMS MONITORING.

Data Bus Buffer

This tri-state bidirectional 8-bit buffer is used to interface the HS-82C55ARH to the system data bus (see Figure 8). Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

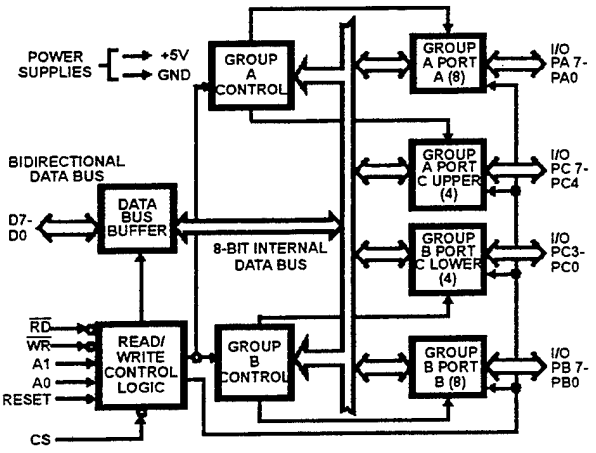


FIGURE 8. BLOCK DIAGRAM DATA BUS BUFFER, READ/WRITE, GROUP A AND B CONTROL LOGIC FUNCTIONS

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfer of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU writes a control word to the HS-82C55ARH. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the HS-82C55ARH.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group - Port A and Port C upper (C7 - C4)

Control Group - Port B and Port C lower (C3 - C0).

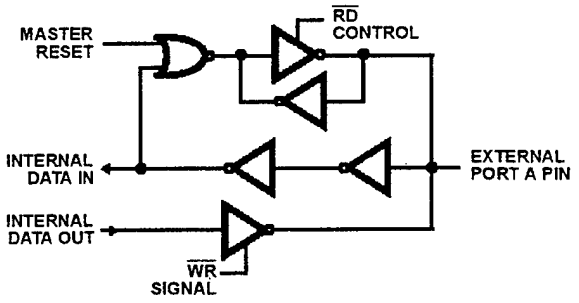
Ports A, B, C

The HS-82C55ARH contains three 8-bit ports (A, B and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the HS-82C55ARH.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus hold devices are present on Port A. See Figure 9A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 9B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B. See Figure 9B.



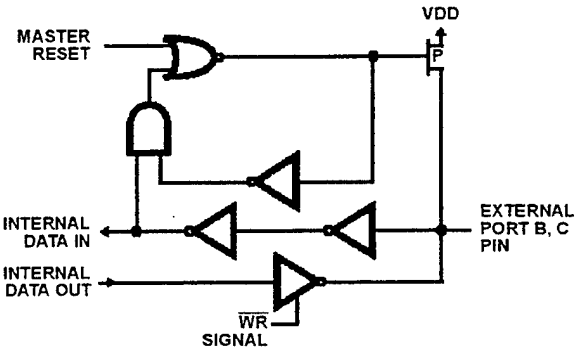


FIGURE 9. I/O PORT CONFIGURATION

Operational Description

Control Word

The data direction and mode of Ports A, B and C are determined by the contents of the Control Word. See Figure 11. The Control Word can be both written and read as shown in Table 1 and 2. During write operations, the function of the Control Word being written is determined by data bit D7. If D7 is low, the data on D0 - D3 will set or reset one of the bits of Port C. See Figure 12. During read Operations, the

Control Word will always be in the format illustrated in Figure 11 with Bit D7 high to indicate Control Word Mode Information.

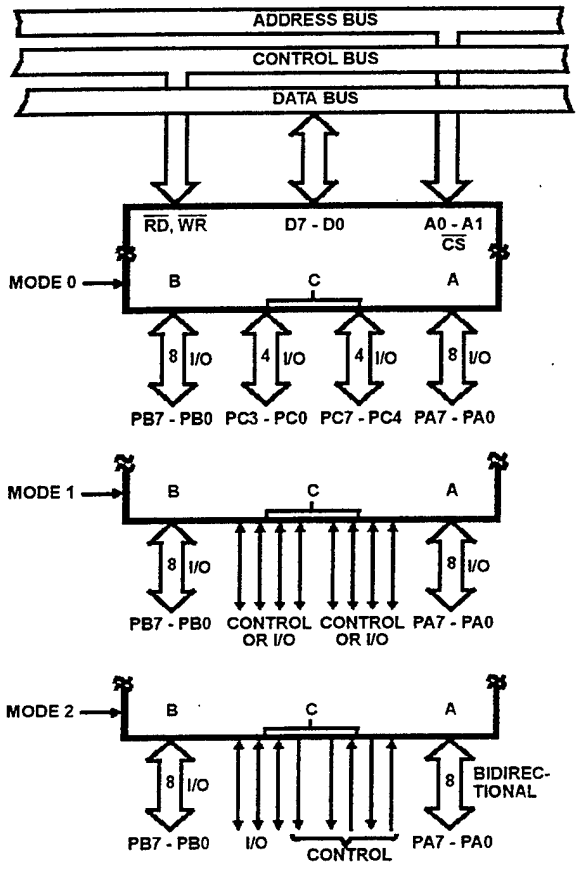


FIGURE 10. BASIC MODE DEFINITIONS & BUS INTERFACE

TABLE 1.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	Port A - Data Bus
0	1	0	1	0	Port B - Data Bus
1	0	0	1	0	Port C - Data Bus
1	1	0	1	0	Control Word - Data Bus

TABLE 2.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus - Port A
0	1	1	0	0	Data Bus - Port B
1	0	1	0	0	Data Bus - Port C
1	1	1	0	0	Data Bus - Control Word

TABLE 3.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	DISABLE FUNCTION
X	X	X	X	1	Data Bus - 3-State
X	X	1	1	0	Data Bus - 3-State

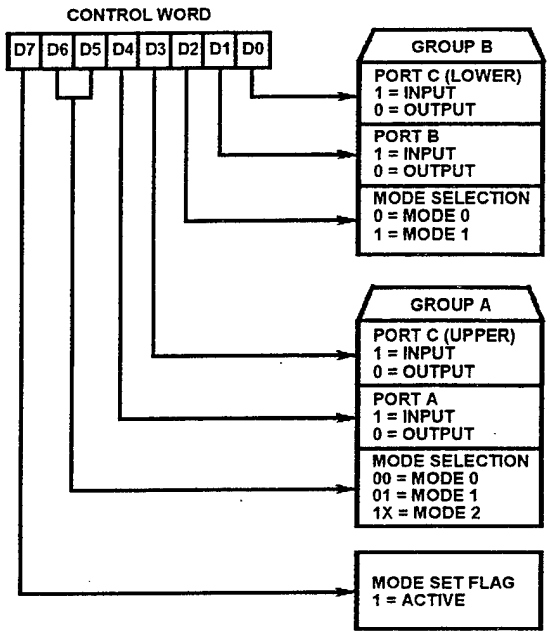


FIGURE 11. MODE SET CONTROL WORD FORMAT

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bidirectional Bus

When the RESET input goes "high", all ports will be set to the input mode with all 24 port lines held at the logic "one" level by internal bus hold devices. After reset, the HS-82C55ARH can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single HS-82C55ARH to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape recorder on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the HS-82C55ARH has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

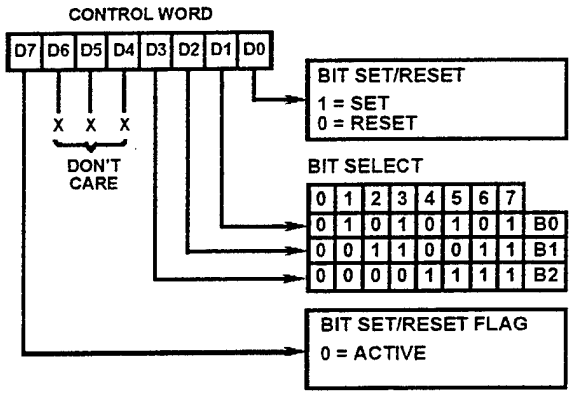


FIGURE 12. BIT SET/RESET CONTROL WORD FORMAT

Single Bit/Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. See Figure 12. This feature reduces software requirements in control-based applications.

Interrupt Control Functions

When the HS-82C55ARH is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enable by setting or resetting the associated INTE flip-flop, using the Bit Set/Reset function of Port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition:

(BIT-SET) - INTE is SET - Interrupt enable.

(BIT-RESET) - INTE is RESET - Interrupt disable.

NOTE: All mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the three ports. No handshaking it required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible

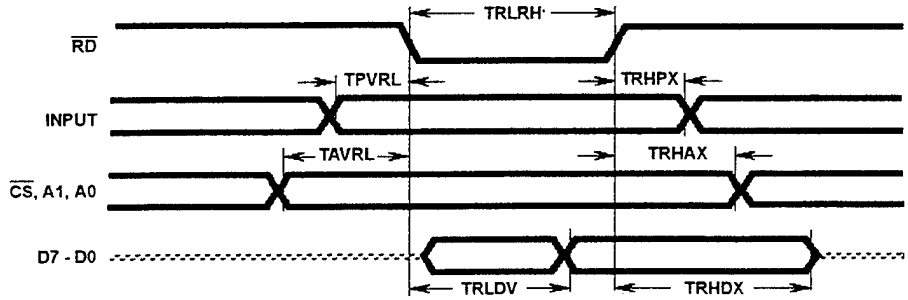


FIGURE 13. MODE 0 (BASIC INPUT)

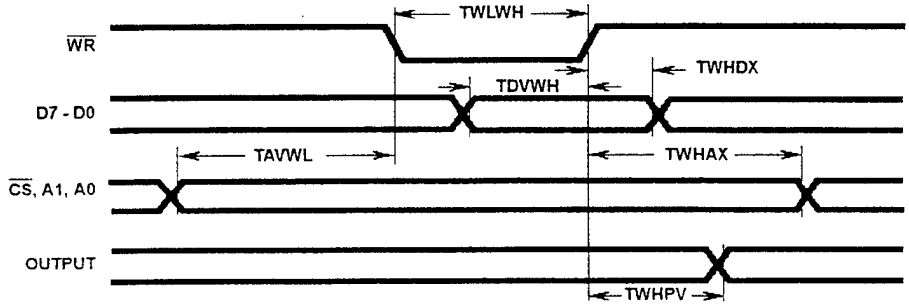


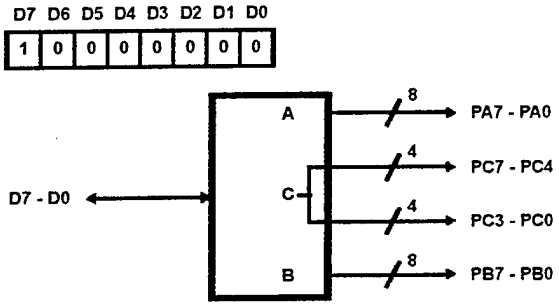
FIGURE 14. MODE 0 (BASIC OUTPUT)

Mode 0 Port Definition

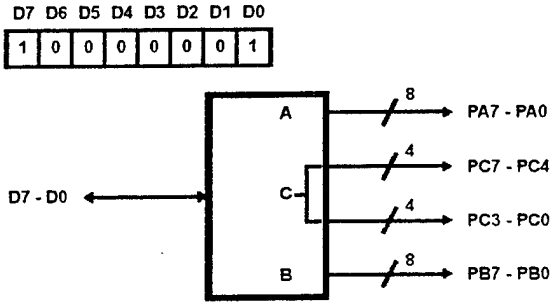
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (UPPER)	NO.	PORT B	PORT C (LOWER)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

Mode 0 Configurations

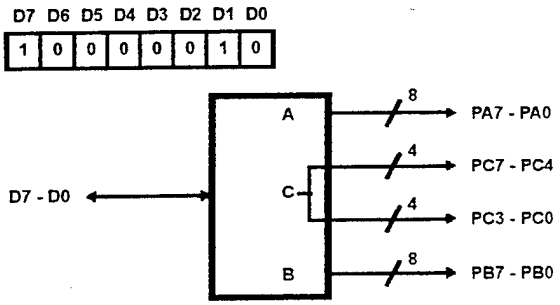
CONTROL WORD #0



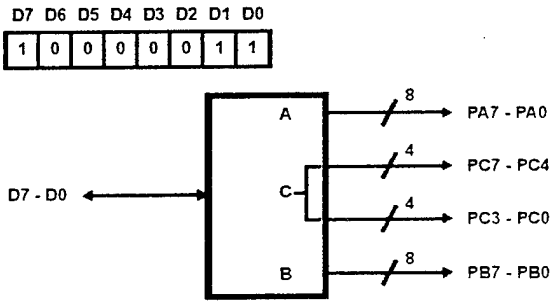
CONTROL WORD #1



CONTROL WORD #2



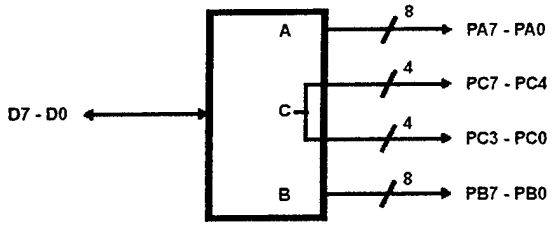
CONTROL WORD #3



Mode 0 Configurations (Continued)

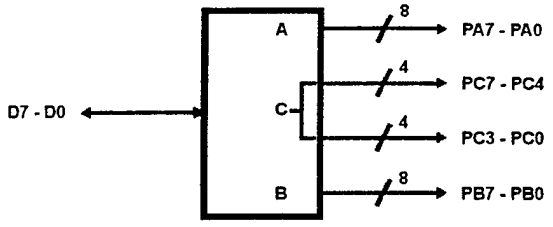
CONTROL WORD #4

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	0	0



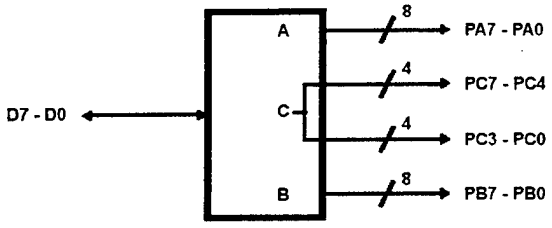
CONTROL WORD #5

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	0	0	1



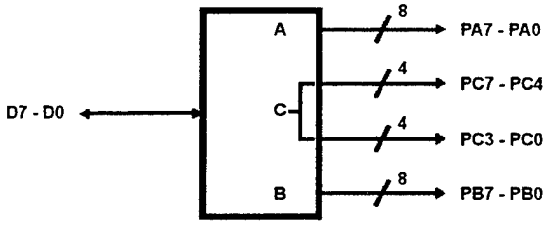
CONTROL WORD #6

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	0



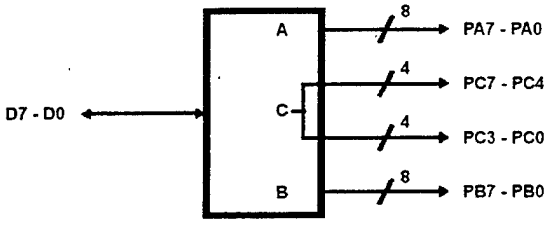
CONTROL WORD #7

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	0	1	1



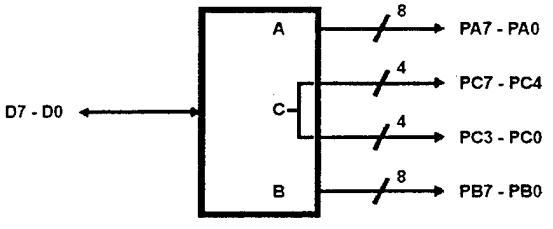
CONTROL WORD #8

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0



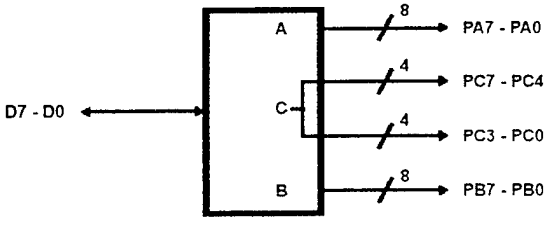
CONTROL WORD #9

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	1



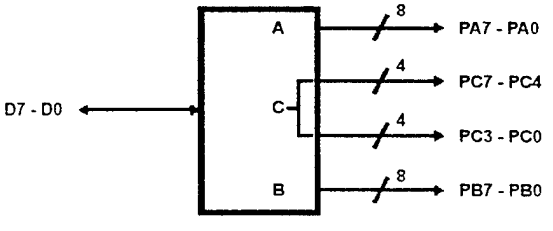
CONTROL WORD #10

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	0



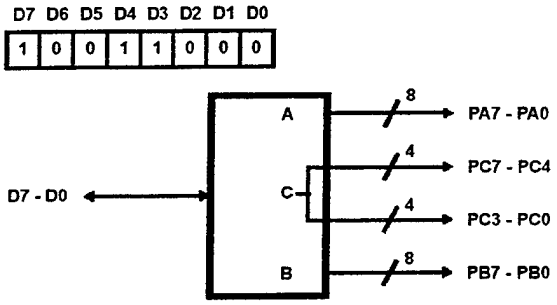
CONTROL WORD #11

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	1	1

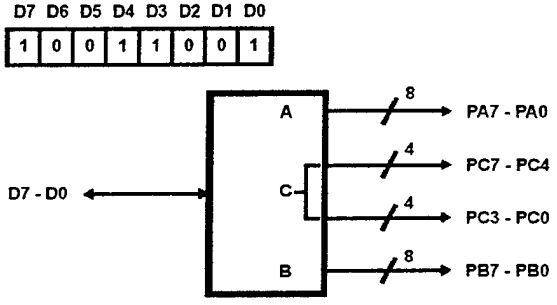


Mode 0 Configurations (Continued)

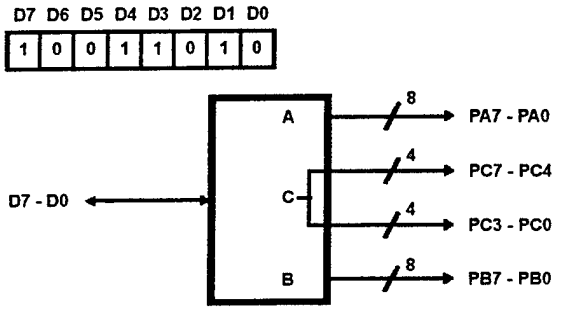
CONTROL WORD #12



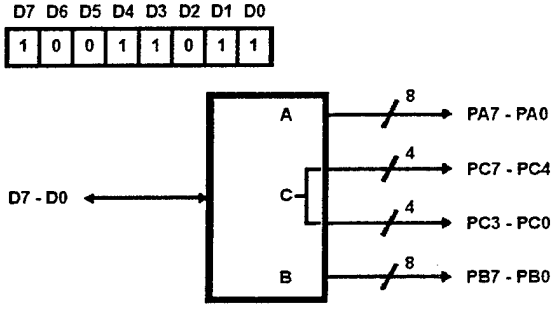
CONTROL WORD #13



CONTROL WORD #14



CONTROL WORD #15



Operating Modes

Mode 1 (Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In Mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the rising edge of $\overline{STB}$ and reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by Bit Set/Reset of PC4.

INTE B

Controlled by Bit Set/Reset of PC2.

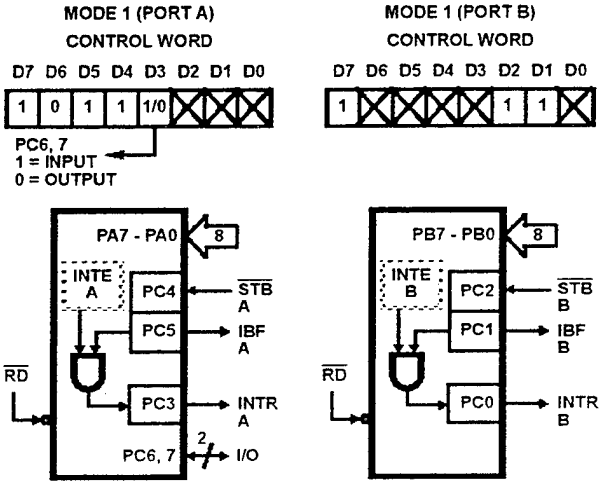


FIGURE 15. MODE 1 INPUT

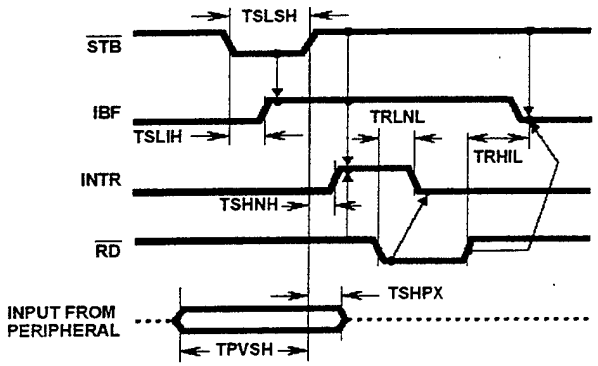


FIGURE 16. MODE 1 (STROBED INPUT)

Output Control Signal Definition

OBF (Output Buffer Full F/F)

The OBF output will go "low" to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the port at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF. See Note 1. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

ACK (Acknowledge Input)

A "low" on this input informs the HS-82C55ARH that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data. See Note 1.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set by the rising edge of ACK and reset by the falling edge of WR.

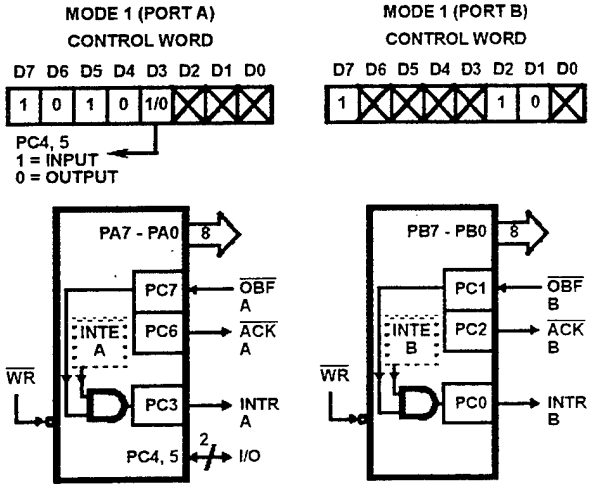


FIGURE 17. MODE 1 OUTPUT

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

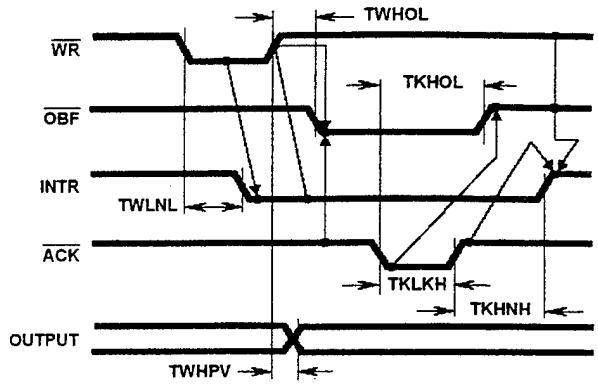


FIGURE 18. MODE 1 (STROBED OUTPUT)

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generate an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

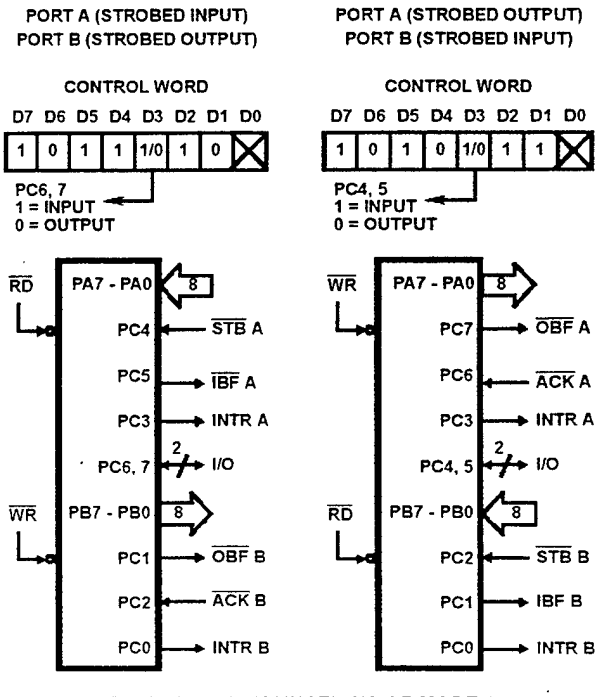


FIGURE 19. COMBINATIONS OF MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bidirectional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bidirectional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request)

A high on this output can be used to interrupt the CPU for both input or output operations. INTR will be set either by the rising edge of $\overline{ACK}$ (INTE1 = 1) or the rising edge of $\overline{STB}$ (INTE2 = 1). INTR will be reset by the falling edge of $\overline{WR}$ (if previously set by the rising edge or $\overline{ACK}$), the falling edge of $\overline{RD}$ (if previously set by the rising edge of $\overline{STB}$), or the falling edge of $\overline{WR}$ when immediately following a low $\overline{RD}$ pulse or the falling edge of $\overline{RD}$ when immediately following a low $\overline{WR}$ pulse (if previously set by the rising edges of both $\overline{ACK}$ and $\overline{STB}$).

Output Operations

$\overline{OBF}$ (Output Buffer Full)

The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge)

A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$)

Controlled by Bit Set/Reset of PC6.

Input Operations

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF)

Controlled by Bit Set/Reset of PC4.

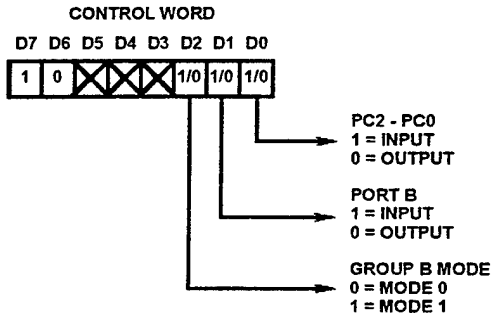


FIGURE 20. MODE CONTROL WORD

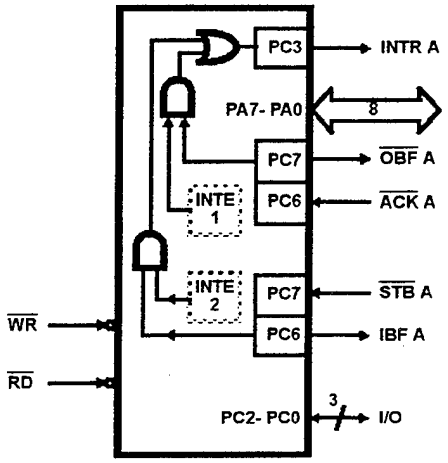
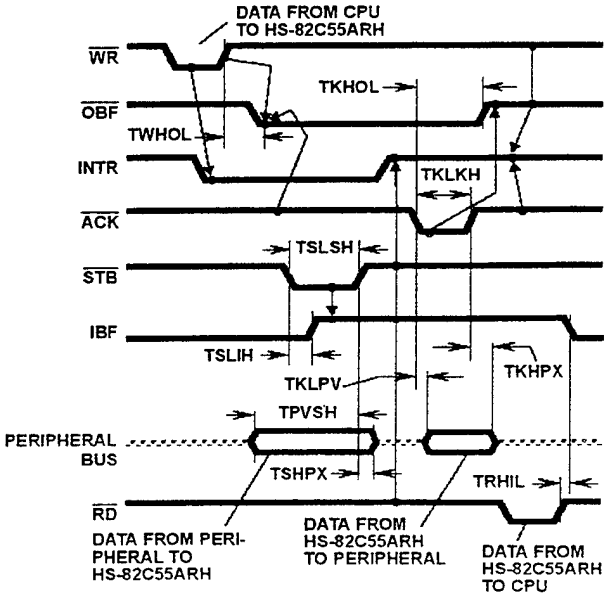


FIGURE 21. MODE 2 (BIDIRECTIONAL)



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

FIGURE 22. MODE 2 (BIDIRECTIONAL)

MODE DEFINITION SUMMARY

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA0	In	Out	In	Out	←	
AP1	In	Out	In	Out	←	
PA2	In	Out	In	Out	←	
PA3	In	Out	In	Out	←	
PA4	In	Out	In	Out	←	
PA5	In	Out	In	Out	←	
PA6	In	Out	In	Out	←	
PA7	In	Out	In	Out	←	
PB0	In	Out	In	Out	-	Mode 0 or Mode 1 Only
PB1	In	Out	In	Out	-	
PB2	In	Out	In	Out	-	
PB3	In	Out	In	Out	-	
PB4	In	Out	In	Out	-	
PB5	In	Out	In	Out	-	
PB6	In	Out	In	Out	-	
PB7	In	Out	In	Out	-	
PC0	In	Out	INTR B	INTR B	I/O	
PC1	In	Out	IBF B	$\overline{OBF}$ B	I/O	
PC2	In	Out	$\overline{STB}$ B	$\overline{ACK}$ B	I/O	
PC3	In	Out	INTR A	INTR A	INTR A	
PC4	In	Out	$\overline{STB}$ A	I/O	$\overline{STB}$ A	
PC5	In	Out	IBF A	I/O	IBF A	
PC6	In	Out	I/O	$\overline{ACK}$ A	$\overline{ACK}$ A	
PC7	In	Out	I/O	$\overline{OBF}$ A	$\overline{OBF}$ A	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 25.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C fare not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 25.

INPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
I/O	I/O	IBFA	INTEA	INTRA	INTEB	IBFB	INTRB
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBFA}$	INTEA	I/O	I/O	INTRA	INTEB	$\overline{OBFB}$	INTRB
GROUP A					GROUP B		

FIGURE 23. MODE 1 STATUS WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
$\overline{OBFA}$	INTE1	IBFA	INTE2	INTRA	X	X	X
GROUP A					GROUP B		

NOTE: (Defined by Mode 0 or Mode 1 Selection)

FIGURE 24. MODE 2 STATUS WORD FORMAT

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status (Figures 23 and 24)

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

INTERRUPT ENABLE FLAG*	POSITION	ALTERNATE PORT C PIN SIGNAL (MODE)
INTE B	PC2	$\overline{ACK}$B (Output Mode 1) or STBB (Input Mode 1)
INTE A2	PC4	$\overline{STB}$A (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}$A (Output Mode 1 or Mode 2)

FIGURE 25. INTERRUPT ENABLE FLAGS IN MODES 1 AND 2

Metallization Topology

DIE DIMENSIONS:
3420µm x 4350µm x 485µm ± 25µm

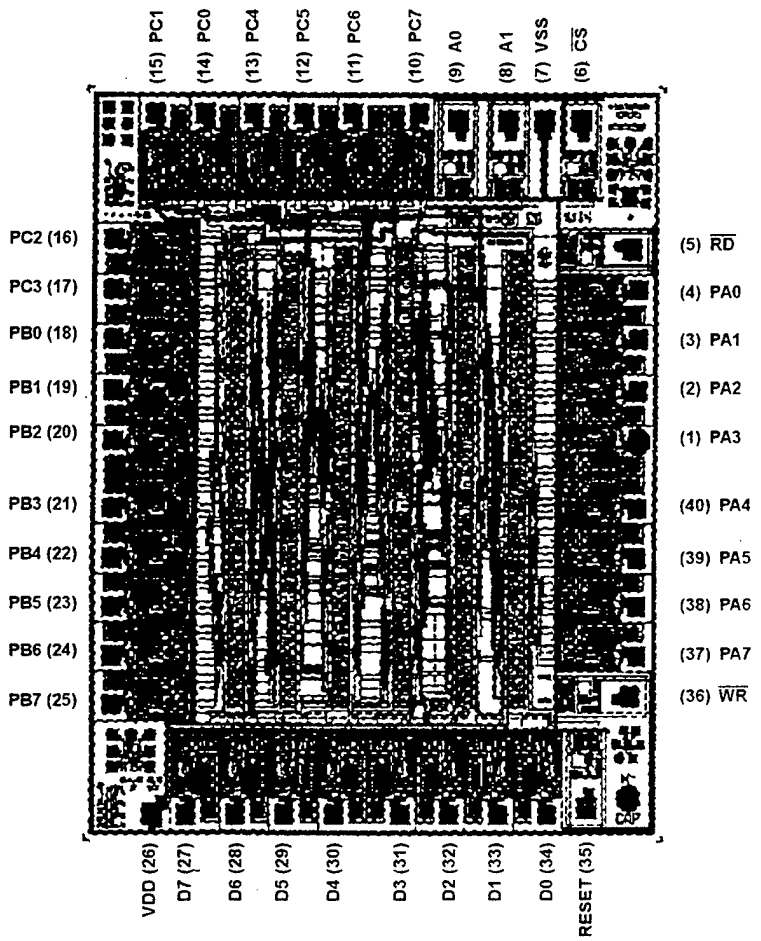
METALLIZATION:
Type: Al/Si
Thickness: 11kÅ ± 2kÅ

GLASSIVATION:
Type: SiO2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
7.7×10^4 A/cm^2

Metallization Mask Layout

HS-82C55ARH



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